Information obtained from all these prototype works, when combined with the knowledge base from this paper, can catalyze cross-layer research in the area of *SOSPh* interconnects design, which can enable the widespread adoption of *SOSPh* platform for realizing extreme-scale on-chip and off-chip communication architectures.

7 Overheads and Challenges

To compare the footprint area of SOS and SOI variants of CLOS PNoC architecture from Table 3, *SOIPh* MR has footprint area of 78μm^2, whereas the footprint areas for SOS-I, SOS-II and SOS-III MRs are 177 μm^2, 707 μm^2 and 708 μm^2 respectively. The footprint area of a 1cm long rectilinear *SOIPh* waveguide is 4500μm^2, whereas the footprint area of 1cm long rectilinear *SOSPh* waveguide is 9700μm^2. In terms of CLOS PNoC architecture, the total footprint area for SOI-based CLOS PNoC architecture is 0.4 mm^2, whereas the footprint area for SOS-I, SOS-II, and SOS-III based CLOS PNoC architectures are 3.1 mm^2, 2.3 mm^2 and 2.4 mm^2, respectively. This comparison clearly shows that SOS links/PNoCs have higher footprint area compared to SOI links/PNoCs.

Note that the traditional fiber optics systems for inter-cluster, inter-datacenter, and long-haul networks still running on O, L and C optical bands. In contrast, *SOSPh* platform operates with wavelengths between 2.5μm-4μm. Therefore, additional specialized equipment and support are needed to introduce *SOSPh* interconnects in this established hierarchy, which is likely to incur extra cost. Nevertheless, it is worth bearing this extra cost, especially considering the energy and performance benefits of *SOSPh* platform shown here.

8 Conclusions

Conventional SOI-based photonic interconnects have limited bandwidth-energy scalability due to the optical non-linear effects in silicon, especially the two-photon-absorption (TPA) effect. In this paper, we presented silicon-on-sapphire (SOS) device platform as a solution to the scalability limitations of SOI-based interconnects. We developed new compact models for SOS devices, utilizing which we formulated new guidelines for designing SOS links and PNoCs. Our link-level analysis showed that SOS links can achieve aggregate data rate of >1Tb/s, which is significantly better than SOI links. Our system-level analysis with CLOS PNoC architecture showed that PNoCs that are designed using SOS devices and links can achieve up to 45% lower latency and 37% lower EPB compared to the PNoCs implemented using the conventional SOI devices and links. These promising results prove that SOS-based PNoCs can achieve high-bandwidth data transfers with low latency and greater energy-efficiency, compared to the traditional SOI-based PNoCs.

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