CV-Ishan G Thakkar

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Personal Information

Contact Information

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Professional Experience

2018 – Present	*Assistant Professor* Department of Electrical and Computer Engineering, University of Kentucky, Lexington, KY, USA
2016 – 2018	*Community Coordinator* University Housing, Colorado State University, Fort Collins, CO, USA
2013 – 2018	*Graduate Research and Teaching Assistant* Embedded Systems and High-Performance Computing (EPiC) Lab, Colorado State University, Fort Collins, CO, USA
2012 – 2013	*Graduate Research Assistant* Optoelectronics Research Group, Colorado State University, Fort Collins, CO, USA
Spring/Fall 2011	*Graduate Teaching Assistant* Department of Electrical and Computer Engineering, Colorado State University, Fort Collins, CO, USA
Summer 2011	*Research Intern* Microwave Systems Laboratory, Colorado State University, Fort Collins, CO, USA
2010	*Ad-hoc Lecturer* Department of Computer Engineering, Venus International College of Technology, Gujarat, India
2009	*Project Intern* Peach Technovations Pvt. Ltd., Gandhinagar, Gujarat, India

Education

August 2018 — *Ph.D. in Electrical Engineering*
Colorado State University, Fort Collins, CO, USA
Dissertation: Design and Optimization of Emerging Interconnection and Memory Subsystems for Future Manycore Architectures
Advisor: Sudeep Pasricha

May 2013 — *M.S. in Electrical Engineering*
Colorado State University, Fort Collins, CO, USA
Thesis: A plastic total internal reflection-based photoluminescence device for enzymatic biosensors
Advisor: Kevin Lear

June 2009 — *B.E. in Electronics and Communication Engineering*
L.D. College of Engineering, Ahmedabad, Gujarat, India

Awards and Honors

2020 — ***Best Paper Award Honorary Selection***
ACM Great Lakes Symposium on VLSI (GLSVLSI), "LORAX: Loss-Aware Approximations for Energy-Efficient Silicon Photonic Networks-on-Chip," September, Virtual Event.

2017 — ***Ph.D. Forum Travel Grant***
IEEE/ACM/SIGDA Design Automation Conference (DAC),
Austin, Texas, USA, June 2017.

2017 — ***Travel Award***
Graduate Student Council of Colorado State University, To Present a Peer-Reviewed Research Paper at the IEEE International Conference on VLSI Design (VLSID), Hyderabad, India.

2017 — ***Best Journal Paper Award Candidate***
IEEE Transactions on Multi-Scale Computing Systems (TMSCS), “3D-ProWiz: An Energy-Efficient and Optically-Interfaced 3D DRAM Architecture with Reduced Data Access Overhead”

2016 — ***Best Paper Award***
ACM System Level Interconnect Prediction (SLIP) Workshop, “A Comparative Analysis of Front-End and Back-End Compatible Silicon Photonic On-Chip Interconnects,” Austin, Texas, USA.

2016 — ***Best Paper Award Finalist***
IEEE International Symposium on Quality Electronic Design (ISQED), “Process Variation Aware Crosstalk Mitigation for DWDM based Photonic NoC Architectures,” Santa Clara, California, USA.

Professional Society Membership

2018-Present	IEEE Member
2018-Present	ACM Member
2016-2018	ACM Student Member
2014-2018	IEEE Student Member

Research Activities

Research Interest Statement

My research broadly focuses on the design and optimization of unconventional (More-than-Moore) architectures and technologies for energy-efficient, reliable, and secure computing, for a wide scope of platforms including embedded systems, internet-of-things (IoT), and high-performance computing systems. More specific More-than-Moore technology interests include (1) Silicon photonics; (2) Optical computing; (3) Neuromorphic computing; (4) In-memory computing; (5) Stochastic computing; (6) Monolithic 3D (M3D) integration; (7) Polymer and transparent conductive oxides based photonic devices and sensors. More specific topics of interest include: 1) design of on-chip and inter-chip networks, 2) memory architecture design, 3) 3D integrated chip design, 4) design with emerging technologies, e.g., silicon photonics, phase change materials, spintronics, 5) self-adaptive and cognitive architectures, 6) manycore hardware security, 7) high-speed optical interfaces, 8) resource management techniques, and 9) optoelectronic/photonic sensors and communication devices.

Note

After each publication (article/paper/chapter/patent/poster/presentation/talk) listed in different categories below, one of the following code letters is used to indicate the nature of the review process. This code letter is followed by a double asterisk (**) for publications with one of my graduate/undergraduate students, and an asterisk (*) for publications with my thesis advisors. A double asterisk (**) after an author's name indicates that the author is my student at UK.

- **W** Full publication reviewed by one or more anonymous referees; involves multiple stages of revisions and rebuttals
- **W⁻⁻** Full publication reviewed by more than one anonymous peers; rigorous review similar to W category; low acceptance rate (15%-30%); publishing in this category is often harder than publishing in W category because of low acceptance rate and as no revisions are allowed
- **X** Full publication reviewed by editor or by conference organizing committee ` invited
- **Y** Only abstract is reviewed
- **Z⁺** Not reviewed at the time of submission/acceptance, but judged by peers, editor or conference committee, etc., afterwards
- **Z** Not reviewed

Research Book Chapters

[BC4] – Ishan Thakkar, Sai Vineel Reddy Chittamuru, Varun Bhat, *Sairam Sri Vatsavai***, Sudeep Pasricha, "Securing Silicon Photonic NoCs Against Hardware Attacks", to appear, Springer Book on Network-on-Chip Security and Privacy, 2021. **(X)****

[BC3] – Ishan Thakkar, Sai Vineel Reddy Chittamuru, Varun Bhat, *Sairam Sri Vatsavai***, Sudeep Pasricha, "Hardware Security in Emerging Photonic Network-on-Chip Architectures," Silicon Photonics for High Performance Computing and Beyond, *to appear, Springer Book on Emerging Computing, June 2020*. **(X)****

[BC2] – Ishan Thakkar, Sudeep Pasricha, *Venkata Sai Praneeth Karempudi***, Sai Vineel Reddy Chittamuru, "Exploring Aging Effects in Photonic Interconnects for High-Performance Manycore Architectures," Silicon Photonics for High Performance Computing and Beyond, CRC Press/Taylor & Francis Group, *to appear in December 2019*. **(X)****

[BC1] - Sudeep Pasricha, Sai Vineel Reddy Chittamuru, Ishan Thakkar, "Enhancing Process Variation Resilience in Photonic NoC Architectures," Photonic Interconnects for Computer Systems – Understanding and Pushing Design Challenges, River Publishers, June 2017. **(X)***

Archived Papers

[AP1] – *Supreeth Mysore Shivanandamurthy***, Ishan Thakkar, Sayed Ahmad Salehi, "ODIN: A Bit-Parallel Stochastic Arithmetic Based Accelerator for In-Situ Neural Network Processing in Phase Change RAM," arXiv:2103.03953, January 2020.

Peer-Reviewed Journal Publications (Full-Papers)

[J8] – Febin Sunny, Asif Mirza, Ishan Thakkar, Mahdi Nikdast, Sudeep Pasricha, "ARXON: A Framework for Approximate Communication over Photonic Networks-on-Chip", accepted in IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 2021. **(W)***

[J7] – Sai Vineel Reddy Chittamuru, Ishan Thakkar, Sudeep Pasricha, *Sairam Sri Vatsavai***, Varun Bhat, "Exploiting Process Variations to Secure Photonic NoC Architectures from Snooping Attacks," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2020. **(W)****

[J6] – Sai Vineel Reddy Chittamuru, Ishan Thakkar, Sudeep Pasricha, "LIBRA: Thermal and Process Variation Aware Reliability Management in Photonic Networks-on-Chip," accepted for publication in IEEE Transactions on Multi-Scale Computing Systems (TMSCS), June 2018. **(W)***

[J5] – Ishan Thakkar, Sudeep Pasricha, "DyPhase: A Dynamic Phase Change Memory Architecture with Symmetric Write Latency and Restorable Endurance," IEEE Transactions on Computer Aided Design (TCAD), vol. 37, no. 9, pp. 1760-1773, September 2018. **(W)***

[J4] – Sai Vineel Reddy Chittamuru, Ishan Thakkar, Sudeep Pasricha, "HYDRA: Heterodyne Crosstalk Mitigation with Double Microring Resonators and Data Encoding for Photonic NoCs," IEEE Transactions on Very Large-Scale Integration (TVLSI), vol. 26, no. 1, pp. 168-181, January 2018. **(W)***

[J3] – Ishan Thakkar, Sudeep Pasricha, "3D-ProWiz: An Energy-Efficient and Optically-Interfaced 3D DRAM Architecture with Reduced Data Access Overhead," IEEE Transactions on Multi-Scale Computing Systems (TMSCS), vol. 1, no. 3, pp. 168-184, September 2015. **(Best Paper Candidate)** **(W)***

[J2] – Ishan Thakkar, Sudeep Pasricha, "3D-WiRED: A Novel WIDE I/O DRAM with Energy-Efficient 3-D Bank Organization," IEEE Design & Test, vol. 32, no. 4, pp. 71-80, August 2015. **(W)***

[J1] – Ishan Thakkar, Kevin L Lear, Jonathan Vickers, Brian Heinze and Kenneth Reardon, "A plastic total internal reflection photoluminescence device for enzymatic biosensing," Lab Chip, vol. 13, no. 34, pp. 4775-4783, December 2013. **(W)***

Peer-Reviewed Conference Publications (Full-Papers; 15-30% acceptance rate)

[C24] – Sairam Sri Vatsavai, Ishan Thakkar, "Silicon Photonic Microring Based Chip-Scale Accelerator for Delayed Feedback Reservoir Computing," IEEE 34th International Conference on VLSI Design & 20th International Conference on Embedded Systems (VLSID 2021), February, 2021. **(W⁻⁻)****

[C23] – *Chao-Hsuan Huang***, Ishan Thakkar, "Mitigating the Latency-Area Tradeoffs for DRAM Design with Coarse-Grained Monolithic 3D (M3D) Integration," IEEE International Conference on Computer Design (ICCD), October, 2020. **(W⁻⁻)****

[C22] – *Sairam Sri Vatsavai***, *Venkata Sai Praneeth Karempudi***, Ishan Thakkar, "PROTEUS: Rule-Based Self-Adaptation in Photonic NoCs for Loss-Aware Co-Management of Laser Power and Performance," IEEE/ACM International Symposium on Networks-on-Chip (NOCS), September, 2020. **(W⁻⁻)****

[C21] – *Febin Sunny*, Asif Mirza, Ishan Thakkar, Sudeep Pasricha, Mahdi Nikdast, "LORAX: Loss-Aware Approximations for Energy-Efficient Silicon Photonic Networks-on-Chip," ACM Great Lakes Symposium on VLSI (GLSVLSI), May, 2020. **(Best Paper Award Honorary Selection)** **(W⁻⁻)****

[C20] – *Venkata Sai Praneeth Karempudi***, *Sairam Sri Vatsavai***, Ishan Thakkar, "Redesigning Photonic Interconnects with Silicon-on-Sapphire Device Platform for Ultra-Low-Energy On-Chip Communication," ACM Great Lakes Symposium on VLSI (GLSVLSI), May, 2020. **(W⁻⁻)****

[C19] – *Venkata Sai Praneeth Karempudi***, Ishan Thakkar, "Mitigating Inter-Channel Crosstalk Non-Uniformity in Microring Filter Arrays of Wavelength-Multiplexed Photonic NoCs," ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), New York, NY, USA, October 2019. **(W⁻⁻)****

[C18] – *Supreeth Mysore Shivanandamurthy**, Ishan Thakkar, Sayed Ahmad Salehi, "A Scalable Stochastic Number Generator for Phase Change Memory Based In-Memory Stochastic Processing," ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), New York, NY, USA, October 2019. **(W⁻⁻)****

[C17] - *Chao-Hsuan Huang**, Ishan Thakkar, "Mitigating Write Disturbance in Phase Change Memory," ACM/IEEE International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), New York, NY, USA, October 2019. **(W⁻⁻)****

[C16] - Ishan Thakkar, Sai Vineel Reddy Chittamuru, Sudeep Pasricha, "Mitigating the Energy Impacts of VBTI Aging in Photonic Networks-on-Chip Architectures with Multilevel Signaling," IEEE Workshop on Energy-efficient Networks of Computers (E2NC): from the Chip to the Cloud, Pittsburgh, PA, USA, October 2018. **(X)***

[C15] - Sudeep Pasricha, Sai Vineel Reddy Chittamuru, Ishan Thakkar, Varun Bhat, "Securing Photonic NoCs from Hardware Trojans," IEEE/ACM International Symposium on Networks-on-Chip (NOCS), Torino, Italy, October 2018. **(X)***

[C14] - Sudeep Pasricha, Sai Vineel Reddy Chittamuru, Ishan Thakkar, "Cross-Layer Thermal Reliability Management in Silicon Photonic Networks-on-Chip," ACM Great Lakes Symposium on VLSI (GLSVLSI), Chicago, IL, USA, May 2018. **(X)***

[C13] - Sai Vineel Reddy Chittamuru, Ishan Thakkar, Varun Bhat, Sudeep Pasricha, "SOTERIA: Exploiting Process Variations to Enhance Hardware Security with Photonic NoC Architectures," IEEE/ACM Design Automation Conference (DAC), San Francisco, CA, USA, June 2018. (acceptance rate: 168/691 = 24.3%) **(W--)***

[C12] - Ishan Thakkar, Sai Vineel Reddy Chittamuru, Sudeep Pasricha, "Improving the Reliability and Energy-Efficiency of High-Bandwidth Photonic NoC Architectures with Multilevel Signaling," IEEE/ACM International Symposium on Networks-on-Chip (NOCS), Seoul, South Korea, October 2017. (acceptance rate: 14/44 = 31.8%) **(W--)***

[C11] - Sai Vineel Reddy Chittamuru, Ishan Thakkar, Sudeep Pasricha, "Analyzing Voltage Bias and Temperature Induced Aging Effects in Photonic Interconnects for Manycore Computing," ACM System Level Interconnect Prediction Workshop (SLIP), Austin, TX, USA, June 2017. **(W--)***

[C10] - Ishan Thakkar, Sudeep Pasricha, "DyPhase: A Dynamic Phase Change Memory Architecture with Symmetric Write Latency," IEEE International Conference on VLSI Design (VLSID), Hyderabad, India, January 2017. (acceptance rate: 71/292 = 24.3%) **(W--)***

[C9] - Ishan Thakkar, Sai Vineel Reddy Chittamuru, Sudeep Pasricha, "Mitigation of Homodyne Crosstalk Noise in Silicon Photonic NoC Architectures with Tunable Decoupling," ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), Pittsburgh, PA, USA, October 2016. (acceptance rate: 21/80 = 26.3%) **(W--)***

[C8] - Ishan Thakkar, Sai Vineel Reddy Chittamuru, Sudeep Pasricha, "Run-Time Laser Power Management in Photonic NoCs with On-Chip Semiconductor Optical Amplifiers," IEEE/ACM International Symposium on Networks-on-Chip (NOCS), Nara, Japan, August 2016. **(W--)***

[C7] - Ishan Thakkar, Sai Vineel Reddy Chittamuru, Sudeep Pasricha, "A Comparative Analysis of Front-End and Back-End Compatible Silicon Photonic On-Chip Interconnects," ACM System Level Interconnect Prediction Workshop (SLIP), Austin, TX, USA, June 2016. **(Best Paper Award)** **(W--)***

[C6] - Sai Vineel Reddy Chittamuru, Ishan Thakkar, Sudeep Pasricha, "PICO: Mitigating Heterodyne Crosstalk Due to Process Variations and Intermodulation Effects in Photonic NoCs," IEEE/ACM Design Automation Conference (DAC), Austin, TX, USA, June 2016. (acceptance rate: 152/876=17%) **(W--)***

[C5] - Sai Vineel Reddy Chittamuru, Ishan Thakkar, Sudeep Pasricha, "Process Variation Aware Crosstalk Mitigation for DWDM based Photonic NoC Architectures," IEEE International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, USA, March 2016. (acceptance rate: 36.3%) **(Best Paper Award Finalist)** **(W--)***

[C4] - Ishan Thakkar, Sudeep Pasricha, "Massed Refresh: An Energy-Efficient Technique to Reduce Refresh Overhead in Hybrid Memory Cube Architectures," IEEE International Conference on VLSI Design (VLSID), Kolkata, India, January 2016. (acceptance rate: 86/339 = 25.4%) **(W^{--})***

[C3] - Ishan Thakkar, Sudeep Pasricha, "A Novel 3D Graphics DRAM Architecture for High-Performance and Low-Energy Memory Accesses," IEEE International Conference on Computer Design (ICCD), New York, NY, USA, Oct 2015. (acceptance rate: 83/269=30.8%) **(W^{--})***

[C2] - Sudeep Pasricha, Ishan Thakkar, "Re-architecting DRAM memory systems with 3D Integration and Photonic Interfaces," Memory Architecture and Organization Workshop (MeAOW), Oct 2014. **(X)***

[C1] - Ishan Thakkar, Sudeep Pasricha, "3D-Wiz: A Novel High Bandwidth, Optically Interfaced 3D DRAM Architecture with Reduced Random Access Time," IEEE International Conference on Computer Design (ICCD), Seoul, South Korea, Oct 2014. (acceptance rate: 64/207=30.9%) **(W^{--})***

Peer-Reviewed PhD Forum

[PF1] - Ishan Thakkar, "Design and Optimization of Emerging Network-Memory Subsystems for Future Manycore Architectures," at the ACM/IEEE Design Automation Conference (DAC) PhD Forum, Austin, TX, USA, June 2017. **(W^{--})**

Conference Tutorials

[TU1] - A. T-Sanial, Sudeep Pasricha, P. Pande, K. Chakrabarty, "3D Integration: Quo Vadis?" Full day tutorial at IEEE Design Automation and Test in Europe Conference, (DATE), Mar 2017.
My Contributions: helped with the preparation of the material presented by Sudeep Pasricha.

Invited Seminar/Conference Talks

[T7] - Ishan Thakkar, "VBTI Aging: Yet Another Critical Design Challenge for Microring Resonator Based Silicon Photonic Interconnects," Silicon Photonics for High-Performance Computing Workshop (SPHPC), Fort Collins, CO, USA, May 2018. **(Z)**

[T6] - Ishan Thakkar, "Design and Optimization of Interconnection and Memory Subsystems for Future Manycore Computing," Department of Electrical and Computer Engineering, University of Massachusetts Dartmouth, Dartmouth, MA, USA, April 2018. **(Z^{+})**

[T5] - Ishan Thakkar, "Design and Optimization of Interconnection and Memory Subsystems for Future Manycore Computing," Department of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR, USA, March 2018. **(Z^{+})**

[T4] - Ishan Thakkar, "Design and Optimization of Interconnection and Memory Subsystems for Future Manycore Computing," Department of Electrical and Computer Engineering, University of Kentucky, Lexington, KY, USA, February 2018. **(Z^{+})**

[T3] - Ishan Thakkar, "Design and Optimization of Interconnection and Memory Subsystems for Future Manycore Computing," Computer Engineering, Rochester Institute of Technology, Rochester, NY, USA, February 2018. **(Z^+)**

[T2] – Ishan Thakkar, "Design and Optimization of Interconnection and Memory Subsystems for Future Manycore Computing," Department of Electrical Engineering and Computer Science, University of Kansas, Lawrence, KS, USA, December 2017. **(Z^+)**

[T1] - Sudeep Pasricha, Ishan Thakkar, "Re-architecting DRAM memory systems with 3D Integration and Photonic Interfaces," Memory Architecture and Organization Workshop (MeAOW), October, 2014. **(X)***

Conference Poster Presentations

[CP8] - *Venkata Sai Praneeth Karempudi***, Ishan Thakkar, "Mitigating Inter-Channel Crosstalk Non-Uniformity in Microring Filter Arrays of Wavelength-Multiplexed Photonic NoCs," ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), New York, NY, USA, October 2019. **(W^{--})****

[CP7] - *Supreeth Mysore Shivanandamurthy***, Ishan Thakkar, Sayed Ahmad Salehi, "A Scalable Stochastic Number Generator for Phase Change Memory Based In-Memory Stochastic Processing," ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), New York, NY, USA, October 2019. **(W^{--})****

[CP6] - *Chao-Hsuan Huang***, Ishan Thakkar, "Mitigating Write Disturbance in Phase Change Memory," ACM/IEEE International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), New York, NY, USA, October 2019. **(W^{--})****

[CP5] - Ishan Thakkar, "Design and Optimization of Emerging Network-Memory Subsystems for Future Manycore Architectures," in PhD Forum at the ACM/IEEE Design Automation Conference (DAC), Austin, TX, USA, June 2017. **(W^{--})**

[CP4] - Ishan Thakkar, Sai Vineel Reddy Chittamuru, Sudeep Pasricha, "Mitigation of Homodyne Crosstalk Noise in Silicon Photonic NoC Architectures with Tunable Decoupling," ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), Pittsburgh, PA, USA, October 2016. **(W^{--})***

[CP3] - Ishan Thakkar, Sai Vineel Reddy Chittamuru, Sudeep Pasricha, "Run-Time Laser Power Management in Photonic NoCs with On-Chip Semiconductor Optical Amplifiers," IEEE/ACM International Symposium on Networks-on-Chip (NOCS), Nara, Japan, August 2016. **(W^{--})***

[CP2] - Sai Vineel Reddy Chittamuru, Ishan Thakkar, Sudeep Pasricha, "PICO: Mitigating Heterodyne Crosstalk Due to Process Variations and Intermodulation Effects in Photonic NoCs," IEEE/ACM Design Automation Conference (DAC), Austin, TX, USA, June 2016. **(W^{--})***

[CP1] - Ishan Thakkar, Sudeep Pasricha, "A Novel 3D Graphics DRAM Architecture for High-Performance and Low-Energy Memory Accesses," IEEE International Conference on Computer Design (ICCD), New York, NY, USA, October 2015. **(W^{--})***

Research Posters or Presentations (Non-Conference)

[P5] – *Venkata Sai Praneeth Karempudi***, Ishan Thakkar, "Mitigating Inter-Channel Crosstalk Non-Uniformity in Microring Filter Arrays of Wavelength-Multiplexed Photonic NoCs," ECE Research Symposium, University of Kentucky, Lexington, KY, USA, April 2020. **(Z+)****

[P4] – *Chao-Hsuan Huang***, Ishan Thakkar, "Mitigating the Latency-Area Tradeoffs for DRAM Design with Coarse-Grained Monolithic 3D (M3D) Integration," ECE Research Symposium, University of Kentucky, Lexington, KY, USA, April 2020. **(Z+)****

[P3] – *Chao-Hsuan Huang***, Ishan Thakkar, "Mitigating Write Disturbance in Phase Change Memory Architectures," ECE Research Symposium, University of Kentucky, Lexington, KY, USA, April 2019. **(Z+)****

[P2] - Ishan Thakkar, Sai Vineel Reddy Chittamuru, Sudeep Pasricha, "A Comparative Analysis of Front-End and Back-End Compatible Silicon Photonic On-Chip Interconnects," ACM/IEEE Design Automation Conference Work in Progress (WIP), Austin, TX, USA, June 2016. **(X)***

[P1] - Ishan Thakkar, Sudeep Pasricha, "Improving the Performance and Power Efficiency of Memory with 3D Stacking and High-Bandwidth Optical Interfacing," CSU Ventures Innovation Forum, Fort Collis, CO, USA, April 2016. **(Y)***

Patents Submitted

[PAT2] - U.S. patent application serial no. 16/434420, titled "Hardware Security for Photonic Communication Architectures," filed on 6/7/2019.
Inventors: Sai Vineel Reddy Chittamuru, Sudeep Pasricha, Ishan Thakkar

[PAT1] - U.S. provisional patent application serial no. 61/970,155, titled "Low Cost Chemical and Biochemical Sensor," filed on 3/25/14.
Inventors: Ishan Thakkar, Kevin L Lear, Kenneth F Reardon

Educational Activities

Current Ph.D. Thesis Students (Advisor/Co-Advisor)

August 2019- *Sairam Sri Vatsavai*
Research Topic: Cognitive Memory and NoC Architectures
Research Posters and Presentations: -
Journal and Conference Publications: C20, C22, C24, J7

May 2019- *Supreeth Mysore Shivanandamurthy*
Research Topic: Nonvolatile Processing in Memory
Research Posters and Presentations: CP7
Journal and Conference Publications: C18, AP1

January 2019- *Venkata Sai Praneeth Karempudi*
Research Topic: Design and Optimization of Silicon Photonic NoCs
Research Posters and Presentations: CP8, P5
Journal and Conference Publications: C19, C20, C22

Current M.S. Thesis Students (Advisor)

December 2018- *Chao-Hsuan Huang*
Research Topic: Design of Main Memory Architectures with Emerging Technologies
Research Posters and Presentations: P3, CP6, P4
Journal and Conference Publications: C17, C23

Current B.S. Students (Advisor)

April 2020- *Bobby Bose*
Research Topic: DRAM Reliability and In-DRAM Computing
Research Posters and Presentations: -
Journal and Conference Publications: -

M.S. Project Students Graduated (Supervisor)

May 2018 *Varun Kilenje*
Colorado State University
Advisor: Prof. Sudeep Pasricha
Final Project: Exploiting Process Variation to Enhance Hardware Security in Photonic NoC Architectures
Publications: C15, J7

December 2017 *Rohit Kudre*
Colorado State University
Advisor: Prof. Sudeep Pasricha

Final Project: Reducing Refresh Overhead in Hybrid Memory Cube Architectures with Efficient Power Delivery and Awareness to Inter-Tier Nonuniformity

May 2017 — *Sai Kiran Koppu*
Colorado State University
Advisor: Prof. Sudeep Pasricha
Final Project: Analysis of Front-End and Back-End compatible Silicon Photonic On-Chip Interconnects

Teaching and Evaluation at University of Kentucky

(Department course evaluation average: 4.0 out of 5.0)

Semester	***Course***	***Evaluation***
Spring 2021	EE/CS/CPE 480: Computer Architecture	-
Fall 2020	EE685-001: Digital Computer Structure	-
Spring 2020	EE599-003: Low Power and Secure Computing	-
Spring 2020	EE699-003: Low Power and Secure Computing	-
Fall 2019	EE685-001: Digital Computer Structure	4.9 out of 5.0
Spring 2019	EE599-003: HW-SW Design for IoT Systems	4.5 out of 5.0
Spring 2019	EE699-003: HW-SW Design for IoT Systems	4.7 out of 5.0
Fall 2018	EE685-001: Digital Computer Structure	-

Other Teaching Experience

April 2018 — *Guest Lecture*
On the topic of "On-Chip Communication and Interconnection Networks On-Chip (NoCs)" in a graduate level course, Computer Organization and Design, at Colorado State University

October 2017 — *Guest Lecture*
On the topic of "On-Chip Communication: Buses and Networks-on-Chip (NoCs)" in a graduate level course, Hardware-Software Design for Embedded Systems at Colorado State University

September 2016 — *Guest Lecture*
On the topic of "On-Chip Communication: Buses and Networks-on-Chip (NoCs)" in a graduate level course, Hardware-Software Design for Embedded Systems, at Colorado State University

August 2016 — *Guest Lecture*
On the topic of "System C Tutorial" in a graduate level course, Hardware-Software Design for Embedded Systems, at Colorado State University

October 2015	*Guest Lecture* On the topic of "On-Chip Communication: Buses and Networks-on-Chip (NoCs)" in a graduate level course, Hardware-Software Design for Embedded Systems, at Colorado State University
Fall 2015	*Teaching Assistant* For a graduate level course, Computer Organization and Design
Fall 2011	*Teaching Assistant* Taught assembly level programming to junior students in an undergraduate course, Introduction to Microprocessors
Spring 2011	*Teaching Assistant* For a graduate level course, Engineering Risk Analysis
Summer 2010	*Expert Lectures* On "Preparing for Quantitative Aptitude Tests" to senior-level undergraduate students at Genesis Consultants, Institute for Management and Foreign Studies (IMFS), India
Fall 2009 Spring 2010	*Ad-hoc Lecturer* Taught "Basics of programming using C and C++" and "Elements of Electrical Engineering" to sophomore undergraduate students at the Venus International College of Technology (VICT), Gandhinagar, Gujarat, India
September 2010	*Expert Lecture* On the topic of "Robust Hardware Design for Remotely Controlled Robocars" to undergraduate students at the Venus International College of Technology (VICT), Gandhinagar, Gujarat, India

Student Awards

2020	*Student Participation Support*, IEEE IGSCC 2020 (*Supreeth Shivanandamurthy*)
2020	*Student Participation Support*, IEEE IGSCC 2020 (*Venkata Sai Praneeth Karempudi*)
2020	*Student Participation Support*, IEEE IGSCC 2020 (*Sairam Sri Vatsavai*)
2020	*Student Participation Support*, IEEE IGSCC 2020 (*Chao-Hsuan Huang*)
2019	*Travel Award*, ACM/IEEE ESWEEK 2019 (*Chao-Hsuan Huang*)
2019	*Travel Award*, ACM/IEEE ESWEEK 2019 (*Supreeth Mysore Shivanandamurthy*)
2019	*Travel Award*, ACM/IEEE ESWEEK 2019 (*Venkata Sai Praneeth Karempudi*)

Professional Development (Participation)

March 2019	*NSF CAREER Workshop* Proposal Development Office, University of Kentucky Research Foundation, Lexington, KY, USA
June 2017	*DAC Early Career Workshop* IEEE/ACM Design Automation Conference (DAC), Austin, TX, USA
June 2017	*Entering Mentoring* Certificate course at Colorado State University, Fort Collins, CO, USA
May 2017	*NSF Day Workshop* University of Wyoming, Laramie, WY, USA
April 2015	*Interacting with Federal Funding Agencies* Seminar at the Information Science and Technology Center (ISTeC), Colorado State University, Fort Collins, CO, USA

Professional and University Service

Editorial Activities

2021-2022 Associate Editor
IEEE Technical Committee on Very Large Scale Integration (TCVLSI) Newsletter

2021-2022 Review Editor
Frontiers in Neuroscience Journal, Editorial Board of Neuromorphic Engineering

Proposal Review Panels

2020 National Science Foundation

Conference/Workshop Organizing Committee (General Chair)

2020 Workshop on Computing with Unconventional Technologies (CUT),
Co-located with International Green and Sustainable Computing (IGSC) Conference

2019 Workshop on Computing with Unconventional Technologies (CUT),
Co-located with International Green and Sustainable Computing (IGSC) Conference

Conference/Workshop Organizing Committee (Other Chaired Positions)

2021 *Workshop Chair*
IEEE International Green and Sustainable Computing (IGSC) Conference

2020 *Virtual Conference Management Chair*
IEEE International Green and Sustainable Computing (IGSC) Conference

2020 *Panel Chair, Moderator*
IEEE/ACM International Workshop on Network on Chip Architectures (NoCArc)

2020 *Web Chair,*
IEEE/ACM International Symposium on Networks-on-Chip (NOCS)

2019 *Web Chair*
IEEE/ACM International Symposium on Networks-on-Chip (NOCS)

2017 *Publicity Chair*
IEEE International Green and Sustainable Computing (IGSC) Conference

Conference Technical Program Committee (TPC) Member

2021 IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)

2021	IEEE/ACM International Symposium on Networks-on-Chip (NOCS)
2021	IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)
2021	IEEE International Symposium on Quality Electronic Design (ISQED)
2021	ACM/IEEE Design Automation Conference (DAC)
2020	ACM SIGDA / IEEE CEDA Design Automation Conference (DAC) PhD Forum
2020	IEEE International Green and Sustainable Computing (IGSC) Conference
2020	IEEE/ACM International Symposium on Networks-on-Chip (NOCS)
2020	ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)
2020	ACM Great Lakes Symposium on VLSI (GLSVLSI)
2020	ACM/IEEE Design Automation Conference (DAC)
2019	IEEE International Green and Sustainable Computing (IGSC) Conference
2019	IEEE International Symposium on Embedded Many-core Systems-on-Chip (MCSoC)
2019	IEEE/ACM International Symposium on Networks-on-Chip (NOCS)
2019	ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)
2019	IEEE International Conference on VLSI Design
2018	IEEE International Green and Sustainable Computing (IGSC) Conference
2018	IEEE International Conference on VLSI Design
2017	IEEE International Green and Sustainable Computing (IGSC) Conference

Activities as a Journal Reviewer/Conference External Reviewer

2021-Present	IEEE Embedded Systems Letters
2020	IEEE Computer Society Annual Symposium on VLSI (ISVLSI)
2020-Present	IEEE Computer Architecture Letters
2020-Present	IEEE Transactions on Computers (TC)

2019-Present	ACM Transactions on Architecture and Code Optimization (TACO)
2019	IEEE/ACM Design and Automation Conference (DAC)
2018-Present	Elsevier Journal of Parallel and Distributed Computing
2018-Present	Springer Design Automation for Embedded Systems
2018	IEEE/ACM Design and Automation Conference (DAC)
2017	IEEE/ACM Design Automation Conference (DAC)
2016-Present	IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
2016	IEEE/ACM International Symposium on Networks-on-Chip (NOCS)
2016-Present	ACM Transactions on Embedded Computing Systems
2015-Present	IEEE Transactions on Multi-Scale Computing Systems
2015-Present	IEEE Transactions on Very Large-Scale Integration Systems
2015-Present	ACM Transactions on Design Automation of Electronic Systems (TODAES)
2014-Present	ACM Journal on Emerging Technologies in Computing Systems

Conference Technical Session Chair

2020	IEEE/ACM Design Automation Conference (DAC)
2019	ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)
2019	IEEE/ACM International Symposium on Networks-on-Chip (NOCS)

University, College, and Department Service

2019-2020	Strategic Planning Committee, Electrical and Computer Engineering Department