3D-ProWiz: An Energy-Efficient and Optically-Interfaced 3D DRAM Architecture with Reduced Data Access Overhead

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Abstract—This paper introduces 3D-ProWiz, which is a high-bandwidth, energy-efficient, optically-interfaced 3D DRAM architecture with fine grained data organization and activation. 3D-ProWiz integrates sub-bank level 3D partitioning of the data array to enable fine-grained activation and greater memory parallelism. A novel method of routing the internal memory bus to individual subarrays using TSVs and fanout buffers enables 3D-ProWiz to use smaller dimension subarrays without significant overhead. The use of TSVs at subarray-level granularity eliminates the need to use slow and power hungry global lines, which in turn reduces the random access latency and activation-precharge energy. 3D-ProWiz yields the best latency and energy consumption values per access among other well-known 3D DRAM architectures. Experimental results with PARSEC benchmarks indicate that 3D-ProWiz achieves 41.9 percent reduction in average latency, 52 percent reduction in average power, and 80.6 percent reduction in energy-delay product (EDP) on average over DRAM architectures from prior work.

Index Terms—Fine-grained activation, DRAM, energy-efficiency, fanout buffers

1 INTRODUCTION

In recent years, DRAM latency has not improved as rapidly as DRAM capacity and bandwidth with shrinking technology, owing to the well-known “memory-wall” problem [1]. Continued process technology scaling has enabled commodity memory system solutions to exploit smaller and faster transistors to improve memory capacity and bandwidth. However, the traditional means of improving memory access performance by increasing clock frequency is no longer practical due to increasingly stringent power constraints that limit further frequency scaling. Thus, performance improvements in memory systems today are primarily reliant on latency tolerance techniques such as multi-level caches, row-prefetching, burst-mode access, memory scheduling [2], and memory parallelism [3], [4]. But the performance improvements obtained through these techniques are not expected to scale well for high performance computing systems of the future [5]. Moreover, preserving the minimum standard capacitance of a DRAM cell is becoming increasingly challenging with shrinking feature size [6]. These trends are forcing designers to reinvent DRAM architectures so as to overcome the hurdles in DRAM performance scaling.

Since the emergence of 3D integration technology, 3D-stacked DRAM has been a promising option to alleviate many of the physical limitations of commodity DRAMs. In recent years, several 3D DRAM architectures have been proposed [7], [8], [9], [10], [11], [12], [13], [14], that have exploited high bandwidth through silicon vias (TSVs) to improve memory latency and throughput. Such 3D-stacked DRAM designs require new methods for efficient address and data path routing and 3D cell organization, to realize their full potential and achieve improved memory parallelism and energy-efficiency.

In this paper, first of all we identify the critical elements of a 3D-stacked DRAM architecture that contribute significantly to the overall latency, energy consumption, and die area. Then, we propose 3D-ProWiz, a new 3D DRAM architecture with a photonic interface that tones down the unfavorable effects of the critical DRAM elements to improve access latency and energy consumption characteristics of DRAM subsystem over prior efforts. Our 3D-ProWiz DRAM architecture is an extension of the 3D-Wiz DRAM architecture [11] with notable improvements in the bank floorplan that adhere to pitch-matching rules and awareness of inter-component connections at the subarray level, which makes the manufacturing and implementation of 3D-ProWiz DRAM more feasible. Our key contributions in this paper can be summarized as follows:

- Fine-grained 3D organization of DRAM data array: Bank-level parallelism in a commodity DRAM data array is limited by the total number of banks the data array is partitioned into. A typical DRAM data array is partitioned into 4 to 16 banks. These banks are very large in capacity, ranging from 32 to 256 Mb, and hence they are few in number. To enable higher memory parallelism in 3D-ProWiz, its data array (DRAM rank) is divided into 512 smaller banks. A very large number of banks greatly increase bank-level parallelism in 3D-ProWiz. In addition, we conservatively estimate a reasonable non-zero...
value of the two banks activation window (tTAW) constraint, which limits the power rail noise to a safe level while exploiting increased bank-level parallelism. Moreover, each bank in 3D-ProWiz is many-fold smaller than a commodity bank and acts independently, which greatly reduces data access energy.

- **TSV-based internal memory bus**: In 3D-stacked DRAM, the address and data buses are routed to each die layer in the vertical direction using TSVs. After reaching a die they are routed to the edges of individual banks along 2D routing paths. These 2D routing paths (or global lines) and global peripheral circuits (decoders, repeaters and drivers of global lines) incur latency, energy, and area overhead at each die. Contrarily, in 3D-ProWiz DRAM, we make intelligent use of TSVs in conjunction with fanout buffers at finer granularity to route data and address lines to individual subarrays, which eliminates the need to use 2D routing paths and global peripheral circuits at each die. This in turn enables the use of smaller sized banks and subarrays to reduce the overall area, latency, and energy consumption.

- **Reduced access time**: The DRAM access time is a function of the sum of row to column command delay (tRCD) and column command to data out delay (tCAS). For a subarray of interest, the timing constraints tRC and tCAS are proportional to the capacitive loading of wordlines and bitlines respectively, which are increasing functions of the number of columns and number of rows respectively [4]. We reduced the access time of 3D-ProWiz by carefully reducing the number of rows and columns in a subarray so as to not harm the DRAM cell area efficiency compared to the area efficiency of other 3D-stacked DRAM architectures. Moreover, fanout buffers and the TSV-based internal memory bus help further reduce access time in 3D-ProWiz.

- **High-bandwidth photonic interface**: We observed that the conventional electrical interfaces of the DDRx family [16],[33] and differential lane based interfaces [34] cannot support very high bandwidths. So in 3D-ProWiz, we propose using a higher bandwidth, dense wavelength division multiplexing (DWDM) based photonic interface. We also investigated the energy-efficiency of conventional electrical interfaces such as DDR3 [16], LPDDR3 [33], Wide-I/O [17] and differential serial interface [34] in terms of energy-per-byte values and compared it with the energy-efficiency of the proposed photonic interface when used with 3D-ProWiz. The results of this comparison showed that use of a photonic interface with 3D-ProWiz greatly improves throughput and energy-efficiency of the DRAM subsystem.

- **Sensitivity analysis**: We analyzed the sensitivity of our 3D-ProWiz architecture to different address mapping policies and memory scheduling policies for PARSEC benchmarks to determine a combination of policies that achieve the best energy-efficiency in terms of energy-delay product (EDP). We also analyzed the sensitivity of average latency of 3D-ProWiz and other DRAM architectures to different values of the tTAW constraint in an effort to understand the relationship between the tTAW constraint, bank-level memory parallelism, and average latency.

## 2 Background and Motivation

In this section, we briefly discuss the state-of-the-art data array organizations for 3D-stacked DRAMs, and identify the fundamental elements that contribute significantly to the overall DRAM access latency, energy consumption, and die area.

Different organizations of data array differ in the way banks and ranks are stacked and partitioned across the 3D die-stack. Accordingly, the 3D organizations of data array are referred to as coarse-grained or fine-grained rank-level partitioning, or bank-level partitioning [15]. Loh [7] was the first to highlight the potential performance benefits achievable by altering the data array organization for conventional 3D-stacked DRAMs. Previous approaches (prior to [7]) did not fully exploit 3D-stacking technology, as the individual structures inside DRAMs were still 2D. Loh [7] proposed splitting a rank across multiple layers instead of laying out a rank on a single layer, and showed up to 1.75× DRAM performance improvement. Woo et al. [8] proposed the SMART-3D DRAM architecture that used a vertical L2-fetch and write-back network made up of a large array of TSVs to hide the latency behind large data transfers. Kang et al. [9] proposed extending the commodity DDR3 architecture to 3D-DDR3 and showed benefits in energy consumption due to the reduced length of the TSV-based memory bus. The hybrid memory cube (HMC) exploits fine-grained rank-level partitioning to further reduce the access latency and increase memory parallelism [10]. All of these approaches [7], [8], [9], [10] exploit the bandwidth from low-energy vertical TSVs to reduce access latency and/or energy. But, they miss out on the potential of 3D data array organization and TSVs to more aggressively improve performance, reduce access energy, and improve energy-efficiency in DRAM data arrays.

Chen et al. [15] discussed the pros and cons of coarse-grained and fine-grained rank-level partitioning for 3D DRAMs with respect to latency, energy consumption, and area efficiency. For the coarse-grained rank-level cell organization, the inter-bank communication within one rank occurs via 2D routing paths. It is shown that activation energy and latency of the fine-grained design are reduced by 48.5 and 46.9 percent respectively compared to the coarse-grained design, because of the reduced bank size and optimized data path routing in the fine-grained design. The total die area for the fine-grained design reduces by 35.9 percent in spite of a 3.7 percent TSV area overhead. Also, the latency of the internal memory bus is reduced by 62.8 percent for the fine-grained design. The reason behind the improved results for the fine-grained model is that the model utilizes the potential bandwidth of TSVs for inter-bank transfers, which relaxes the need for 2D routing paths for such transfers and alleviates related overheads. From these results, it can be concluded that many of the limitations that arise with DRAM scaling can be overcome by intelligently organizing the data array of 3D-stacked DRAMs.

Recent advancements in TSV-based 3D-stacked DRAM technology have enabled the use of high density TSVs at subarray-level granularity [11],[12],[14], which has enabled
elimination of 2D routing paths (global lines) and provided new opportunities in designing low-power and high bandwidth data organizations. Thakkar and Paricha [11] proposed the 3D-Wiz DRAM architecture for high-performance systems, which eliminates global lines by employing aggressive vertical routing of intra-bank buses using TSVs and fanout buffers. The same authors also proposed the 3D-WiRED DRAM architecture in [12] for use in energy-constrained embedded systems. 3D-WiRED renders high energy-efficiency due to its 3D folded bank organization. To ease implementation of 3D-DRAM architectures that use TSVs at subarray level granularity (such as 3D-Wiz [11], 3D-WiRED [12], and [14]), the layout of a DRAM bank should be designed at subarray level abstraction and it should be aware of inter-component connections. But the layouts of the 3D-Wiz bank [11] and 3D-WiRED bank [12] are unaware of inter-component connections at the subarray level. The 3D-ProWiz DRAM architecture presented in this paper notably extends the 3D-Wiz DRAM architecture [11] with an improved bank floorplan which is aware of inter-component connections at the subarray level. Moreover, we show that by carefully choosing the bank size and an appropriate scheme for TSV based routing of address and data paths, the performance and energy consumption of 3D-ProWiz DRAM can be improved even further.

The organization of the DRAM data array is only one of the limiting factors that affect DRAM performance and energy. The other more fundamental limiting factor is RC loading of the memory access path, which is a function of the number of rows and columns in the accessed subarray. This fact encourages designers to reduce the number of rows and columns in a subarray. But, such a reduction can significantly increase the area overhead, harming overall area efficiency, if it is done without due deliberation. 3D-ProWiz exploits the benefits of intelligent array organization and aggressive vertical routing of address and data paths to counteract this overhead, which enables the use of smaller dimension subarrays.

Additional performance benefits can also be achieved by increasing memory access concurrency inside DRAMs. Zhang et al. proposed 3D-SWIFT [13], which increases bank-level parallelism by employing a large number of small banks. They divide each bank of 3D-SWIFT into 16 smaller banks and operate them independently. However, 3D-SWIFT [13] does not utilize the full potential of high bandwidth TSVs, as it employs the conventional 2D structure of banks. Moreover, aggressive changes made in DRAM organization to achieve higher access concurrency and excessive use of available concurrency may result in suboptimal power consumption, which leads to excessive increase in operating temperature and increased noise in the power delivery network (PDN) of 3D-stacked DRAMs. To keep the power consumption and PDN noise within allowable limits, the bank-level parallelism in 3D-stacked DRAMs is curtailed by the tTAW constraint. In general, the tTAW constraint controls bank-level parallelism by allowing only two bank activates in a rolling window of tTAW time. In 3D-SWIFT [13], the tTAW constraint is over-optimistically estimated to be zero. But, the definition of tTAW constraint implies that increasing the bank-level concurrency of the memory module within power noise limits requires careful design of non-zero tTAW constraint. Therefore, in our 3D-ProWiz architecture we consider a reasonable non-zero value of the tTAW constraint. As the performance and power benefits of memory parallelism also depend on address mapping and scheduling policies, we investigate the sensitivity of 3D-ProWiz to a combination of different address mapping and scheduling policies, as well as different values of tTAW constraint to determine a configuration that achieves the best performance and energy-efficiency.

Lastly, state-of-the-art DRAM modules mainly focus on exploiting concurrency inside the banks (as discussed above) due to limited concurrency outside the banks as a result of bus contention. The contention arises because the internal memory bus and interface bus are shared among all the banks due to pin-bandwidth limitation of the traditional DDR interface [16]. The Wide I/O standard [17], a new JEDEC standard for direct chip-to-chip interfacing of DRAM dies with the processor/controller, has the potential to alleviate these shortcomings for on-chip embedded DRAMs. A Wide I/O DRAM employs a wider interface (typically made of 128 TSVs) to increase the peak bandwidth of memory-to-core interconnect. But the TSV based core-to-memory interface can be realized only for on-chip embedded DRAMs. Its use for off-chip main memory is limited due to pin-bandwidth limitations of off-chip PCB interconnects. In the through-silicon interposer (TSI) interconnect based memory-logic integration, the pin-bandwidth limitation can be alleviated using space-time multiplexed 2.5D I/O channels as done in [38]. The energy-efficiency of such 2.5D I/Os can be improved by adaptively adjusting the I/O output-voltage swing under constraints of both communication power and bit error rate [39]. In contrast, our proposed 3D-ProWiz DRAM targets off-chip interconnect based memory-logic integration and uses intelligent layout of TSV buses and a high speed photonic interface to address the pin-bandwidth limitation.

3 3D-ProWiz Architecture: Overview

In this section, an example DRAM design is described to demonstrate the 3D-ProWiz architecture. As implied from the discussion in Section 2, we aim to use TSVs at subarray-level granularity along with smaller subarrays and greater bank-level parallelism in 3D-ProWiz to achieve greater performance and energy-efficiency without significantly impacting area and cost. As we focus on reducing the capacitive loading of bitlines and wordlines by using smaller subarrays, we avoid time consuming exploration of the subarray design space and assume the organization of bitcells in a smaller subarray of 3D-ProWiz to be based on DRAM solutions found in [14] and in Tezzaron’s DiRAM [18]. Consequently, each subarray within 3D-ProWiz DRAM is a 256 \times 256 arrangement of bitcells and is of size 28 \mu m \times 42 \mu m. This subarray size is smaller than the subarray size (512 \times 512) found in all well-known 3D DRAMs. The following sections describe the 3D-ProWiz architecture in more detail.

3.1 3D-ProWiz Module

In this section, we describe an example design of a 3D-ProWiz module. As shown in Fig. 1a, 8 Gb modules (at 45 nm) of both 3D-Wiz [11] and 3D-ProWiz DRAMs consist of a
stack of four dies, which is divided into four identical ranks. Each rank has eight bankgroups. As shown in Fig. 1b, each bankgroup of a 3D-ProWiz module consists of 64 identical banks. In contrast, each bankgroup of a 3D-Wiz module consists of 128 identical banks, as shown in Fig. 1c. The four DRAM dies of both 3D-Wiz and 3D-ProWiz modules are stacked onto one logic die. For both 3D-Wiz and 3D-ProWiz modules, all of the global control logic (except subarray-level control) of the DRAM is integrated on the logic die. The logic die also contains all of the opto-electrical circuits required to support a bidirectional, 256-bit wide, DWDM photonic data bus between the processor side memory controller and the memory module.

In state-of-the-art 3D-stacked DRAMs, the tTAW power constraint significantly reduces bank-level parallelism in a rank [22]. However, the relatively smaller size of banks in 3D-ProWiz relaxes the tTAW constraint. The internal data bus of 3D-ProWiz is also not shared among banks, but rather each bank has its own data bus made of TSVs. Therefore, bank-level parallelism, which is generally limited by the tTAW constraint and the shared internal memory bus together, is limited by only the tTAW constraint in our 3D-ProWiz module. This improves bank-level parallelism for 3D-ProWiz. The analysis of the tTAW constraint for a 3D-ProWiz module is given in Section 5.

To effectively exploit the high level of parallelism in a 3D-ProWiz module, we use a high bandwidth photonic interface so that a larger number of requests to different banks can be pipelined through the photonic bus. We have found in our studies that the use of a high-bandwidth DWDM based photonic interface significantly improves the throughput and energy-efficiency of the 3D-ProWiz sub-system over the DDR3 [16], LPDDR3 [33] and differential serial interface [34]. The methodology used to perform this analysis along with the detailed results of the analysis and the structure of the proposed photonic interface are described in Section 6.

3.2 Floorplan of 3D-Wiz Bank

To understand the difference between 3D-ProWiz and 3D-Wiz floorplans, firstly the floorplan of a 3D-Wiz bank is briefly revisited here. As described in [11], a 3D-Wiz bank
A 1:8 fanout buffer realized using the design rules of 45 nm technology would have $0.6 \mu m \times 1.6 \mu m$ dimensions [19], which matches with the TSV pitch of 2.4 $\mu m$. Thus, the pitch of all the adjacent circuit blocks in the floorplan of a 3D-Wiz bank match with each other.

### 3.2.2 Inefficient Layout of On-Die Metal Wires

In this section, we explain why the floorplan of a 3D-Wiz bank is not feasible even when the pitch of the adjacent blocks of the bank match with each other. In a 3D-Wiz bank, the on-die metal wires responsible for inter-component interconnection at the subarray level are inefficiently laid out. This makes the manufacturing of 3D-Wiz DRAM infeasible.

Consider Fig. 3, which shows a schematic floorplan of a 3D-Wiz bank with dimensions and metal-wire crossovers. The length of a 3D-Wiz subarray along the X-direction is $38 \mu m$ (including $10 \mu m$ for peripherals), which makes the length of the 3D-Wiz bank to be $304 \mu m$ as there are eight subarrays in a bank along the X-direction. This implies that only 126 TSVs can fit in one row along the X-direction. A 3D-Wiz bank has total 448 TSVs [11] arranged in four rows, in which there are 256 row address TSVs, 64 column address TSVs and 128 data TSVs. As shown in the figure, the TSVs in row2, row3 and row4 have to connect to the fanout buffers through metal-wire crossovers (shown in green color in the figure) partially overlapping the launch pads of at least one row of TSVs. For instance, consider the metal-wire crossover (in green color) that connects a TSV of row3 to a fanout buffer (shown as dark blue triangle). This particular metal-wire crossover overlaps the adjacent TSV of row1 to connect to the fanout buffer, which interrupts the inter-die connection of the overlapped TSV (in the vertical Z-direction) across the die-stack. This results in a very inefficient arrangement that complicates the realization of the 3D-Wiz stack.

Moreover, the 3D-Wiz floorplan shown in Fig. 3 does not account for how the subarray is laid out, which makes the floorplan even more inefficient. In modern subarray structures with folded bitlines, as shown in Fig. 4, the driver of every alternate wordline is on the opposite side of the subarray. So, as shown in Fig. 3, some of the fanout buffers have to connect to the wordline drivers on the other side of the subarray through metal-wire crossovers (shown in yellow color in Fig. 3) that act as global wires overlapping the subarray. This arrangement acts against the original idea of eliminating global wires. In summary, from the preceding discussion it is apparent that the original floorplan of 3D-Wiz is infeasible due to the inefficient use of metal-wire crossovers that connect different components of the bank overlapping TSVs and subarrays.

Consider Fig. 4, which shows a schematic subarray structure with folded bitlines.

### 3.2.3 Alternative Floorplan Design

Alternatively, in a 3D-Wiz bank, TSVs can be arranged on both sides of subarrays to efficiently arrange the connections of fanout buffers to respective wordline drivers without using metal-wire crossings that overlap subarrays. However, this provision would still require TSVs to be arranged in two rows along the X-direction on each side of the subarrays. So, this arrangement does not solve the infeasibility problem, as it would still result in metal-wire crossovers that overlap TSVs hindering their connection to upper layers. Therefore, we modify the floorplan of 3D-Wiz DRAM and derive a more efficient and feasible floorplan as part of our 3D-ProWiz DRAM architecture.

### 3.3 Floorplan of 3D-ProWiz Rank and Bank

In this section, we describe the efficient and feasible floorplan of 3D-ProWiz DRAM. Fig. 5 shows the layout of all the 3D-ProWiz banks and constituent subarrays of a rank on one die layer, along with the TSV bus layout.

As shown in the figure, a rank is partitioned into 512 identical banks (64 banks along Y-axis and eight banks along X-axis). Each bank is folded across four die layers (along Z-axis) and consists of a total of 64 subarrays, 16 subarrays of which are on one layer. All 64 constituent subarrays of a bank are addressed in parallel, and they work in lockstep to serve a cache line. Each subarray has two data lines, which allows a bank to serve a total of 128 data bits in one data burst. Therefore, 3D-ProWiz requires a burst length of 2 to serve a 32 B cache line.

All 16 subarrays belonging to the on-die part of a bank are lined up along the X-direction (Fig. 5), with number of
subarrays along the Y-direction being one. Thus, a bank is 16 subarrays long, one subarray wide and four die layers high. In a rank, a total of eight banks are arranged in the X-direction to form one column of banks. A total of 64 bank-columns are arranged in the Y-direction, which is also the number of banks in a bank-row. Each bank-column has two TSV buses on two opposite sides of the bank. All TSV buses are laid out in the X-direction along the length of a bank-column. All TSVs in a TSV bus are arranged in a single row along the X-direction, thus each TSV bus is eight banks long and one TSV wide. As shown in Fig. 5, each TSV bus is logically partitioned into eight sections. Each bank owns two TSV bus sections, which are located on two opposite sides along the X-direction and are responsible for routing address and data lines to the bank.

Fig. 6 shows a detailed schematic floorplan of the on-die portion of a 3D-ProWiz bank and its TSV bus sections. The 3D-ProWiz floorplan differs from the 3D-Wiz floorplan in several aspects, which makes it more efficient and feasible. A 3D-ProWiz bank is of 4 Mb size and is partitioned across all four DRAM layers. A 3D-Wiz bank consists of total 32 in-unison subarrays, eight of which are on the same die, whereas a 3D-ProWiz bank consists of total 64 subarrays, 16 of which are on the same die. Therefore, we use 1:16 fanout buffers in a 3D-ProWiz bank instead of 1:8 fanout buffers used in the 3D-Wiz bank. Unlike the arrangement of TSVs in the 3D-Wiz bank, the TSVs in the 3D-ProWiz bank are arranged on both sides of the subarrays. The 3D-Wiz DRAM puts the decoders for column address on the logic die, whereas the 3D-ProWiz DRAM puts the decoders for column address on memory dies.

To facilitate efficient connections of TSVs to local wordline drivers on both sides of subarrays without using any metal-wire crossovers that overlap the subarrays, we arranged TSVs to be on both sides of a 3D-ProWiz bank. Also, to avoid metal-wire crossovers that would hinder connections of TSVs to upper layers, TSVs are arranged in a single row on each side of the bank.

As discussed earlier, each in-unison subarray of a 3D-ProWiz bank serves two data bits on a read request, which sets the number of required decoded column address signals to 128. If we assume that the decoders for row address and column address are located on the logic die and decoded address signals are routed to individual subarrays through TSVs, then a 3D-ProWiz bank would have 256 row address TSVs and 128 column address TSVs along with 128 data TSVs (total 512 TSVs). As mentioned earlier and as shown in Fig. 6, the length of a 3D-ProWiz subarray along the X-direction is 38 μm (including 5 μm for peripherals on each side), which makes the length of the 3D-Wiz bank to be 608 μm as there are 16 subarrays in the bank along the X-direction. TSVs are arranged on both sides of a 3D-ProWiz bank, which implies that about half of 512 total TSVs (256 TSVs) have to fit along the 608 μm long TSV bus on each side of the bank. A 608 μm long TSV bus can fit 256 TSVs in a single row at TSV pitch of 2.375 μm, which is 0.025 μm tighter pitch than the standard TSV pitch of 2.4 μm. But, this arrangement does not leave any room for control TSVs, P/G TSVs and any redundant TSVs to cope with TSV failures.

As mentioned earlier, a 3D-ProWiz bank has 128 decoded signals for column address. So, putting the column address decoders on the logic die would require 128 decoded column address lines to be routed to the small area of sense amplifiers and data mux on both sides of each subarray (as shown in Fig. 6) through TSVs using 1:16 fanout buffers and metal wires. Semi-global metal wires have 0.18 μm pitch at 45 nm following a conservative method of area projection [21], which implies that 128 column address wires would occupy 23 μm width in the area of sense amplifiers and data mux. But, the width of the area of sense amplifiers and data mux along the X-axis is just 5 μm (Fig. 6). Thus, accommodating 128 column address wires in the small area of sense amplifiers and data mux is not possible.

Alternatively, we propose to locate the decoders for column address on memory dies along with sense amplifiers and data mux, as shown in Fig. 6. Doing so reduces the number of TSVs required to route the column address to 7. We propose to use seven column address TSVs on each side of the bank. As shown in Fig. 6, a 7-bit address is fed to the column address decoders near each of the 16 subarrays through TSVs using 1:16 fanout buffers and metal wires. The 7-bit address is decoded by the decoder and used to select 1-bit data path through each data mux. Each subarray has one data mux on each side along the X-direction, therefore each subarray has a data I/O width of 2-bits.

An efficient floorplan for the 3D-ProWiz bank, as shown in Fig. 6, renders many benefits. First of all, use of just 14 column address TSVs per bank (seven TSVs on each side) now means that only 199 TSVs (128 row address TSVs, 64 data TSVs and seven column address TSVs), instead of 256 TSVs, have to be fit in 608 μm long TSV bus on each side of the bank. Arranging 199 TSVs in one row occupies only 477.6 μm of the total length at TSV pitch of 2.4 μm. The remaining 130.4 μm on each side can be used for P/G TSVs, control TSVs and redundant TSVs. Moreover, the efficient arrangement of fanout buffers and their connections to TSVs and wordline drivers does not leave behind any metal-wire crossovers that would hinder connections of TSVs to upper layers. Thus, our proposed floorplan of 3D-ProWiz bank adheres to physical design rules and renders efficient design, the implementation of which is practically possible. Note that the fanout buffer stripe (fanout buffers and their metal-wire connections to wordline drivers)
occupies 24.3 μm × 608 μm area per 3D-ProWiz bank, which is not insignificant. But, the greater benefits in performance, power and energy-efficiency obtained with the new floor-plan of a 3D-ProWiz bank outweighs this area overhead. A detailed analysis of area, timings and energy for 3D-ProWiz DRAM is given in Section 4.

4 3D-ProWiz Area, Timing, and Energy Analysis

The area, timing and energy analysis for the 3D-ProWiz architecture was performed by modeling the architecture using CACTI-3DD [15]. A similar analysis was conducted for other well-known 3D DRAM architectures such as the 3D stacked photonic DRAM (3DSPDRAM) [23], 3D DRAM from Samsung (3DSams) [9], and the hybrid memory cube from Micron [10]. The results of the analysis for these architectures were compared with results for 3D-ProWiz and commodity DDR3 DRAM architectures. The models of the aforementioned 3D DRAM architectures were implemented in CACTI-3DD using the technology parameters for the 45 nm node. The 3D DRAM architectures from prior work were chosen to provide a broad coverage of the full spectrum of 3D DRAM designs. For instance, the 3D DRAM architecture from Samsung realizes coarse-grained rank level stacking [9], [15], whereas 3DSPDRAM implements single subarray access (SSA) for a coarse-grained rank-level 3D data array organization [15], [23]. On the other hand, HMC from Micron is designed to exploit fine-grained rank-level partitioning [10], [15]. Even though the 3D-Wiz architecture [11] is infeasible to implement due to its unawareness to the inter-component interconnects at the subarray level, we compare our proposed 3D-ProWiz architecture with 3D-Wiz to highlight the micro-architectural differences between the two architectures in terms of the area, delay and energy values of the corresponding DRAM subsystems.

Table 1 lists the architectural parameters used in CACTI-3DD to model the DRAM designs. For a fair comparison between different architectures, we kept the memory capacity and page size of our memory models constant across all architectures. Table 1 also lists different timing parameters and per access energy/power values obtained from CACTI-3DD based models for the DRAM designs considered in our analysis. 3D-ProWiz demonstrates access latency of 17.3 ns and row cycle time of 23 ns, which are better than other architectures on average by about 49 and 57.2 percent respectively. 3D-ProWiz also yields activation precharge energy of 2 nJ per access, which is better than other architectures on average by 23.6 percent.

We modeled DDR3 [16], LPDDR3 [33], and differential serial interfaces [34], which are used for DDR3, 3DSams and HMC respectively. These interfaces were modeled using the CACTI-IO tool [24]. We use a photonic interface for 3DSPDRAM [23]. We modeled the photonic interface of 3DSPDRAM and 3D-Wiz as well as our proposed photonic interface for 3D-ProWiz using the DSENT tool [25] (see Section 6 for details). As explained in [9], 3DSams uses a low power DDR3 interface where power-hungry redundant circuits including delay-locked-loop (DLL), input buffers, and clock circuitry are eliminated in the slave chips of the 3DSams chip-stack. This design very closely resembles the LPDDR3 interface, which is a low power DDR3 interface without DLLs and input buffers. So we use the LPDDR3 interface for 3DSams in our studies. The refresh cycle time (tRFC) values given in Table 1 are calculated as eight times row cycle time (tRC) and additional recovery time (tREC) of 10 ns. The values of tTAW constraint used in our study are given in Table 1 as well. A detailed analysis of the tTAW constraint is presented in Section 5.

We present detailed breakdowns of delay per access values (obtained from CACTI-3DD, DSENT and CACTI-IO based models) for various DRAMs in Fig. 7. Our goal is to understand how the contribution of some critical architectural components differ across various DRAMs in defining delay per access and energy per access values for these DRAMs. The use of TSV-based internal memory buses

| #ranks | 4 | 4 | 4 | 4 | 4 | 4 |
| #banks/rank | 8 | 8 | 8 | 16 | 4 | 4 |
| #bitlines | 1,024 | 1,024 | 1,024 | 512 | 512 | 1,024 |
| #wordlines | 512 | 512 | 512 | 512 | 512 | 512 |
| Page size | 16 Kb | 16 Kb | 16 Kb | 16 Kb | 8 Kb |
| Bus width | 64 b | 32 b | 8 b | 32 b | 128 b | 128 b |

Timing parameters (ns) [DoI: Delay of Interface]

| tRAS | 36.7 | 33.5 | 33.5 | 32.1 | 17.3 | 20.2 |
| tRC | 54.2 | 51 | 63 | 48 | 23 | 25.1 |
| tTAW | 33 | 51 | 4 | 49 | 16 | 15 |
| tRFC | 443.4 | 418 | 513.6 | 382.6 | 193.8 | 210.8 |
| DoI | 4 | 4 | 16 | 4 | 1 | 2 |

Per access energy values (nJ) [EPA: Energy per Access]

| ActPre E | 3.5 | 3.5 | 0.3 | 3.5 | 2 | 1.4 |
| Read E | 1.9 | 1.4 | 0.4 | 1.1 | 1.8 | 2.1 |
| Interface E | 12.8 | 7.7 | 0.25 | 7.4 | 0.25 | 0.25 |
| EPA | 18.1 | 12.5 | 0.88 | 11.9 | 4.05 | 3.75 |

Power values (mW) [BG: Background]

| BG Power | 2,197.8 | 117.4 | 455 | 1,226.8 | 455 | 455 |
| Refresh | 252.6 | 267.9 | 190.8 | 292.7 | 330.2 | 212.5 |

TABLE 1
Modeling Parameters and Timing, Energy, and Power Values for Various DRAM Architectures

### Notes
- The area, timing and energy analysis for the 3D-ProWiz architecture was performed by modeling the architecture using CACTI-3DD [15]. A similar analysis was conducted for other well-known 3D DRAM architectures such as the 3D stacked photonic DRAM (3DSPDRAM) [23], 3D DRAM from Samsung (3DSams) [9], and the hybrid memory cube from Micron [10].
- The results of the analysis for these architectures were compared with results for 3D-ProWiz and commodity DDR3 DRAM architectures.
- The models of the aforementioned 3D DRAM architectures were implemented in CACTI-3DD using the technology parameters for the 45 nm node.
- The 3D DRAM architectures from prior work were chosen to provide a broad coverage of the full spectrum of 3D DRAM designs.
- For instance, the 3D DRAM architecture from Samsung realizes coarse-grained rank level stacking [9], [15], whereas 3DSPDRAM implements single subarray access (SSA) for a coarse-grained rank-level 3D data array organization [15], [23]. On the other hand, HMC from Micron is designed to exploit fine-grained rank-level partitioning [10], [15].
- Even though the 3D-Wiz architecture [11] is infeasible to implement due to its unawareness to the inter-component interconnects at the subarray level, we compare our proposed 3D-ProWiz architecture with 3D-Wiz to highlight the micro-architectural differences between the two architectures in terms of the area, delay and energy values of the corresponding DRAM subsystems.
- Table 1 lists the architectural parameters used in CACTI-3DD to model the DRAM designs. For a fair comparison between different architectures, we kept the memory capacity and page size of our memory models constant across all architectures.
- Table 1 also lists different timing parameters and per access energy/power values obtained from CACTI-3DD based models for the DRAM designs considered in our analysis. 3D-ProWiz demonstrates access latency of 17.3 ns and row cycle time of 23 ns, which are better than other architectures on average by about 49 and 57.2 percent respectively.
- 3D-ProWiz also yields activation precharge energy of 2 nJ per access, which is better than other architectures on average by 23.6 percent.
- We modeled DDR3 [16], LPDDR3 [33], and differential serial interfaces [34], which are used for DDR3, 3DSams and HMC respectively. These interfaces were modeled using the CACTI-IO tool [24].
- We use a photonic interface for 3DSPDRAM [23]. We modeled the photonic interface of 3DSPDRAM and 3D-Wiz as well as our proposed photonic interface for 3D-ProWiz using the DSENT tool [25] (see Section 6 for details).
- As explained in [9], 3DSams uses a low power DDR3 interface where power-hungry redundant circuits including delay-locked-loop (DLL), input buffers, and clock circuitry are eliminated in the slave chips of the 3DSams chip-stack. This design very closely resembles the LPDDR3 interface, which is a low power DDR3 interface without DLLs and input buffers. So we use the LPDDR3 interface for 3DSams in our studies.
- The refresh cycle time (tRFC) values given in Table 1 are calculated as eight times row cycle time (tRC) and additional recovery time (tREC) of 10 ns. The values of tTAW constraint used in our study are given in Table 1 as well.
- A detailed analysis of the tTAW constraint is presented in Section 5.
- We present detailed breakdowns of delay per access values (obtained from CACTI-3DD, DSENT and CACTI-IO based models) for various DRAMs in Fig. 7. Our goal is to understand how the contribution of some critical architectural components differ across various DRAMs in defining delay per access and energy per access values for these DRAMs.
- The use of TSV-based internal memory buses
reduces the lengths of address and data paths for the 3D-stacked DRAMs such as 3DSams, 3DSPDRAM and HMC compared to DDR3. This results in smaller values of I/O delay and sensing delay for the 3D-stacked DRAMs than DDR3. As shown in Table 1, HMC has 512 bitlines per subarray compared to 1,024 bitlines per subarray in DDR3, 3DSams, and 3DSPDRAM. This results in smaller values of sensing and precharge delays for HMC compared to DDR3, 3DSams and 3DSPDRAM. In the single subarray access architecture of 3DSPDRAM, the entire cache line is serially accessed from only one subarray through an 8-bit wide bank bus, which increases the serialization latency of the 3DSPDRAM interface. This results in larger interface delay for 3DSPDRAM than 3DSams. The use of TSVs at subarray-level granularity further reduces the lengths of address and data paths for 3D-ProWiz compared to other 3D-stacked DRAMs. The effect of this, combined with its smaller subarrays (256 × 256), leads to even smaller values of sensing delay, precharge delay, and restore delay for 3D-ProWiz. Also, the wider data bus (128-bit) in 3D-ProWiz reduces burst length to 2 cycles, lowering interface delay compared to all other DRAMs.

Fig. 8 presents detailed breakdowns of energy per access (obtained from CACTI-3DD, DSENT and CACTI-IO based models) for the various DRAMs. The use of a photonic interface reduces dynamic interface energy for 3DSPDRAM and 3D-ProWiz compared to other DRAMs. In SSA, an entire cache line is served by a single subarray [23], which reduces the granularity of activation for 3DSPDRAM compared to 3DSams, reducing the activation-precharge energy for 3DSPDRAM. The combined effect of smaller subarrays and shorter address and data paths yields smaller values of sensing energy, precharge energy, and restore energy for 3D-ProWiz than DDR3, HMC and 3DSams.

The smaller subarray size (256 × 256) in 3D-ProWiz results in larger areas of wordline drivers and sense amplifiers per DRAM die, compared to all other DRAMs, as smaller size of subarray implies more number of subarrays for a given capacity. Similarly, for HMC, the smaller subarray size (512 × 512) results in larger area of wordline drivers and sense amplifiers than DDR3, 3DSams, and 3DSPDRAM. Due to the

![Fig. 7. Breakdown of delay per access for various DRAMs.](image1)

![Fig. 8. Breakdown of energy per access for various DRAMs.](image2)
combined effect of larger wordline driver area, larger sense amplifier area, and fanout buffer area, 3D-ProWiz DRAM has 9.16 mm² (41.7 percent) more die area than the average die area of all other DRAMs. So the 3D-ProWiz architecture may prove to be relatively costly due to its larger die area. Nonetheless, the significant improvements in access time and energy consumption make 3D-ProWiz a promising architecture candidate for future 3D DRAMs. The higher cost of silicon real estate increases the unit cost of a 3D-ProWiz device. The unit cost of the memory device can be reduced either by reducing the required die area or by reducing the engineering design cost. The layout of a 3D-ProWiz bank (as shown in Fig. 6) is designed using conservative and scalable design rules, which often lead to an oversimplified layout design resulting in larger than required die area as discussed in [19]. The required die area and unit cost of 3D-ProWiz DRAM can be reduced by using more aggressive and process-specific design rules to design the layout of 3D-ProWiz DRAM die. Moreover, the structure of 3D-ProWiz is fairly repetitive at the bank level, which reduces the complexity of the mask-set designs and fabrication process. This in turn reduces the engineering design cost and consequently unit cost of 3D-ProWiz DRAM even further.

The scalability of the 3D-ProWiz bank-size is limited only by the non-scalable size of TSVs, as the size of all other components of the bank except TSVs scale proportionally to the scaled technology node. As implied from Fig. 6, the length covered by the TSVs controls the length of the bank, which suggests that the non-scalability of TSVs affects the bank-length more than the bank-width. This results in inefficient use of available die area, which harms the area efficiency and cost of the DRAM. To cope with this limitation, the number of subarrays along the X-direction in a bank and the fanout strength of the fanout buffers can be changed with the scaling of technology node so that the subarrays and fanout buffers cover the same length as covered by the TSVs.

5 SENSITIVITY ANALYSIS

In this section, we analyze the sensitivity of 3D-ProWiz DRAM to different memory controller policies in order to determine a combination of policies that yield the best performance and energy-efficiency for 3D-ProWiz. We also analyze the sensitivity of the average latency for 3D-ProWiz and other DRAM architectures to different values of the tTAW constraint to better understand the relationship between tTAW constraint, bank-level memory parallelism, and average latency.

5.1 Sensitivity to Memory Controller Policies

The performance and energy-efficiency of a DRAM subsystem not only depends on the DRAM data organization, but also on a number of memory controller policies such as address mapping policy, page mode policy, and scheduling policy.

In modern DRAM devices, the arrays of sense amplifiers can also act as buffers (known as row buffer) that provide temporary data storage [22]. In a DRAM controller that implements the open-page policy, once a row of data is activated in a bank, it is temporarily stored in the row buffer. A row of data, which is temporarily stored in the row buffer, is referred to as a page. In case of open-page policy, spatially and temporally adjacent memory accesses to different columns of the same row/page can be made again with minimal latency, because the row/page is already active in the row buffer. In contrast to the open-page policy, the close-page policy flushes the row buffer after an access finishes. This policy is designed to favor accesses to random locations in memory and optimally supports memory request patterns with low degrees of access locality.

The task of an address mapping scheme (AMS) is to minimize the probability of bank conflicts in temporally adjacent requests and maximize the parallelism in the memory system. To obtain the best performance, the choice of the address mapping scheme is often coupled to the page mode policy of the memory controller. To facilitate the pipelined execution of DRAM commands, the DRAM memory controller uses a scheduling policy that prioritizes DRAM commands based on many different factors, including, but not limited to, the age of the request, the priority of the request, the bank address of the request, the availability of resources to a given request. The reader is directed to [22] for more information on various memory controller policies.

A modern memory controller uses one of the following six address mapping schemes [22], [26]: (1) AMS1 – ch:rank:row:col:bank, (2) AMS2 – ch:row:col:bank:rank, (3) AMS3 – ch:rank:bank:col:row, (4) AMS4 – ch:rank:bank:row:col, (5) AMS5 – ch:row:col:rank:bank, and (6) AMS6 – col:rank:bank:ch. Depending on the address mapping policy, the physical address is resolved into indices in terms of channel ID (ch), rank ID (rank), bank ID (bank), row ID (row) and column ID (col). The address mapping scheme AMS2 is used to maximize the rank level parallelism in the memory system, whereas the scheme AMS6 is used to maximize the channel level parallelism. All the memory systems investigated in this paper are single channel systems with a limited number of ranks (4 ranks/channel). Therefore, the rank level and channel level parallelism that can be leveraged by these systems would be insignificant. Because of this reason, we disregard the address mapping schemes AMS2 and AMS6, and select the remaining four types of address mapping schemes (AMS1, AMS3, AMS4, and AMS5) for our study.

We chose the following two kinds of scheduling policies: (i) Rank-then-Bank-Round-Robin (RBRR) and (ii) First-Come-First-Serve (FCFS). We also analyze the following two page mode policies: (i) Open page (OP) and (ii) close page (CP). We analyzed the sensitivity of 3D-ProWiz DRAM to 16 different combinations of these policies which are listed in Table 3. We performed trace-driven simulation analysis for PARSEC benchmarks using a cycle-accurate DRAM simulator DRAMSim2 [26]. We evaluated energy-delay product values averaged over 12 PARSEC benchmarks [27] for all 16 combinations of policies. The simulation method and environment are described in Section 7 in more detail.

Fig. 9 plots EDP values averaged over 12 PARSEC benchmarks across the 16 combinations of policies. Each column in the figure gives the EDP value averaged over 12 PARSEC benchmarks for the respective combination of policies. The error bars on each column present standard deviation in the EDP value across the benchmarks. EDP values were calculated by multiplying the average-energy with average
latency for memory accesses. Average-energy in each benchmark was calculated by dividing the total energy by total number of transactions. Average-latency was calculated by dividing total latency by the total number of transactions. As evident from the figure, the policy combination RBRR_OP_AMS1 yields the least value of EDP among all policy combinations.

The policy combinations with AMS1 and AMS5 yield less EDP than policy combinations with AMS3 and AMS4. This is because address mapping schemes AMS1 and AMS5 present more opportunity to exploit bank-level parallelism, as in these schemes consecutive memory addresses are mapped to different banks. Increased exploitation of bank-level parallelism results in smaller value of average latency and higher throughput, which in turn results in smaller EDP. Moreover, the policy combinations with RBRR scheduling in general outperform the policy combinations with FCFS scheduling. This is because memory requests face more queuing delay in the case of FCFS scheduling compared to RBRR scheduling. The policy combinations with AMS4 and OP schemes yield smaller EDP in general over the policy combinations with AMS5 and OP schemes. This is because the open page scheme provides higher row buffer hit rate in the case of the AMS4 address scheme than in the case of the AMS5 address scheme.

In summary, as the policy combination RBRR_OP_AMS1 yields the least EDP among all policy combinations, we propose to use this policy combination for 3D-ProWiz DRAM. We did a similar analysis for DDR3, 3DSams, 3DSPDRAM, and HMC as well, and found that policy combination RBRR_OP_AMS1 provides the best EDP values for all of these DRAMs as well. Therefore, we use the policy combination RBRR_OP_AMS1 for all the analysis presented in this paper.

5.2 Sensitivity to tTAW Constraint
In this section, we first estimate reasonable values of the tTAW constraint for all DRAM architectures being studied, before analyzing the sensitivity of average latency for 3D-ProWiz and other DRAM architectures to different values of the tTAW constraint. To prevent the adverse effects of power delivery network noise in commodity 2D DRAMs, the number of activates to different banks in a rolling window of time are limited by the four-bank activation window (tFAW) constraint. In general, the tFAW constraint allows only four bank activates in a rolling window of tFAW time. However, the PDN noise issue is more challenging in 3D DRAMs [9], [40], which makes the tFAW constraint more critical. Therefore, the designers of 3D-stacked DRAMs have conservatively allowed only two bank activates in a rolling window of tTAW time [13], [17]. This new constraint is called two-bank activation window (tTAW).

The tTAW constraint for a given 3D-DRAM module can be estimated if we know the maximum current that can be drawn from the PDN without violating the PDN noise limit. This is because the noise level of a PDN depends on the load current drawn from the PDN and physical locality of consecutive bank activates [9]. The closer the physical locations of banks that are consecutively activated, the more is the PDN noise level. An 8 GB DIMM of DDR4x2400 [36] can draw a maximum of 1.8 A current from its PDN without violating the noise limits. To reduce the noise level in the PDN for 3D-stacked DRAMs, we propose to use $V_{DD}/V_{SS}$ edge TSV pads, as used in [9]. Accordingly, we allocate 10 $V_{SS}$ and 5 $V_{DD}$ pads per bankgroup of the 3D-ProWiz DRAM.

In 3D-stacked DRAMs, the PDN noise level also gets affected by the degree of bank-level concurrency, which is
controlled by tTAW time. This implies that the PDN noise is actually controlled by tTAW time. Here, we present a brief quantitative analysis to show how the PDN noise level is affected by the degree of concurrency. It is implied from the discussion given in [40] that the maximum tolerable IR-drop noise in the PDN network is 75 mV per VDD pad. The resistance of an intermediate level TSV is 730 mOhms as reported in [12], which sets the maximum allowable current draw of 100 mA per VDD pad to limit the IR-drop noise to 75 mV per VDD pad. Considering 5 VDD pads per bankgroup, the assumed design of the PDN can deliver about 500 mA peak current per bankgroup without violating the noise limit. In this case, the 2 nJ activation-precharge energy and 23 ns tRC obtained for a 3D-ProWiz bank (as shown in Table 1) indicates that concurrent refresh operations on six banks of the same bankgroup would draw about 522 mA current ((2 nJ × 6)/23 ns)/1 V = 522 mA) from the VDD pads, which would clearly violate the IR-drop noise limit. Thus, it can be concluded from this discussion that the degree of concurrency, and hence the tTAW time should be optimized to keep the PDN noise to within allowable limits and ensure error-free memory operation. We have assumed nominal operating temperature for the preceding analysis. A detailed analysis of the effect of concurrency on temperature and related analysis of tTAW constraint are beyond the scope of this work.

Now, the VDD at 45 nm technology node is 1 V, thus the peak current of 500 mA corresponds to peak power of 500 mW. Based on this information, we estimate reasonable values of the tTAW constraint for all 3D DRAMs considered in this study, for which the peak power consumption does not exceed 500 mW. For that, we calculate total energy required to access two banks in parallel (2 energy per access) and divide it by 500 mW. The resultant value gives the tTAW constraint in ns. The values of tTAW constraint for all 3D DRAMs given in Table 1 were estimated using this method. We take the tTAW constraint of 33 ns from DDR3-1866 datasheet [37] and use it as tTAW in our model of DDR3 memory for fair comparison of our DDR3 model with other 3D DRAMs that use tTAW instead of tFAW. As shown in Table 1, 3DSPDRAM yields tTAW of 3.6 ns. Such a short tTAW time is justifiable for 3DSPDRAM, as 3DSPDRAM supports SSA architecture in which only one subarray of the target bank is activated while serving a memory request. So, owing to the reasonably large bank size for 3DSGDRAM (implied from the modeling parameters given in Table 1), consecutive activation of two different banks results in activation of two different subarrays that are physically quite far from each other, which in turn results in more stable operation for the 3DSPDRAM data array.

More accurate estimates of the tTAW constraint require detailed circuit-level simulation of the DRAM data array and power delivery network, which is beyond the scope of this paper. But, we believe that it is important to have some insights about the relation of the tTAW constraint with bank-level parallelism and performance. To investigate this relationship we performed sensitivity analysis for the tTAW constraint by varying the tTAW constraint of all DRAMs in a range from 10 to 120 ns with step increase of 10 ns. Thus, the tTAW constraint took 12 different values in the range. Then, we performed trace-driven simulation analysis for PARSEC benchmarks using a cycle accurate DRAM simulator DRAMSim2 [26]. We evaluated access latency values of all DRAM architectures averaged over 12 PARSEC benchmarks for all 12 values of tTAW constraint. The policy combination RBRR_OP_AMS1 was used for all simulations in this study. The simulation method and environment are described in Section 7 with more details.

Fig. 10 plots the average access latency values averaged over 12 PARSEC benchmarks across the 12 tTAW values. Each column in the figure shows access latency value averaged over 12 PARSEC benchmarks for the respective tTAW value of the corresponding DRAM. The error bars on each column represent standard deviation in access latency across benchmarks. The access latency value for each benchmark was calculated by dividing total latency by number of transactions. As evident from the figure, the average latency of 3D-ProWiz increases by 435 ns (2.9× - 585 ns from 150 ns) over 110 ns increase in tTAW, which yields the sensitivity of 2.6 %/ns. Based on similar interpretation of the figure for other DRAMs, the access latencies of 3D-ProWiz, HMC, 3DSPDRAM, 3DSams and DDR3 yield tTAW sensitivity values of 2.6, 0.8, 0.01, 0.2 and 0.2 %/ns respectively. 3DSams and DDR3 yield about the same amount of sensitivity to tTAW. From Table 1, it is observed that 3DSams and DDR3 have row cycle times (tRC) of 51 and 54 ns respectively. The tRC of DDR3 is about 5 percent larger than 3DSams. On the other hand, the tRC of 3DSPDRAM is 63 ns, which is about 24 percent greater than the tRC of 3DSams. From Fig. 10 it can be observed that 3DSPDRAM has low access latency sensitivity to tTAW values. Intuitively, these results imply that, for a DRAM subsystem, the sensitivity of access latency to tTAW is inversely proportional to the row cycle time of the DRAM.

In contrast, the sensitivity to tTAW for HMC is much larger than 3DSams in spite of HMC having only 5 percent smaller value of row cycle time (48 ns). However, HMC has more number of banks than 3DSams (see Table 1), which naturally increases the bank-level parallelism of HMC compared to 3DSams regardless of the tTAW constraint. Due to this reason, HMC access latency is much more sensitive to tTAW values than 3DSams. This implies that the sensitivity of access latency to tTAW is directly proportional to the number of banks in a DRAM. Moreover, among all the DRAM architectures under study, 3D-ProWiz has the smallest tRC of 23 ns and the largest number of banks (512 banks/ rank), which results in the highest value of tTAW sensitivity for 3D-ProWiz. For a system that is relatively more sensitive to tTAW, even a small deviation from the optimal
tTAW constraint (minimal value of tTAW) may result in much larger degradation of performance. For such systems, it is very important to have as small tTAW value as possible, by designing a robust PDN that is less prone to noise.

In conclusion, we have shown that for a given DRAM sub-system, the sensitivity of access latency to tTAW constraint is directly proportional to the number of banks and inversely proportional to the row cycle time. Therefore, it is very important to design a robust PDN, which is less prone to noise and has more relaxed tTAW constraint, for a 3D DRAM sub-system with relatively small tRC and large bank count.

6 Modeling and Analysis of High Bandwidth Photonic Interface

In this section, we first discuss the maximum theoretical bandwidth achievable with 3D-ProWiz and justify the use of a high bandwidth photonic interface. Then we describe the functionality of the logic die that supports this interface. Lastly, we investigate the energy-efficiency of the proposed photonic interface in terms of energy-per-byte values for PARSEC benchmarks and compare it with several conventional electrical interface structures such as DDR3 [16], LPDDR3 [33], Wide-I/O [17] and differential serial interface [34].

6.1 Bandwidth Analysis

As discussed earlier, bank-level parallelism, which is generally limited by the tTAW constraint and the shared internal memory bus together, is limited by only the tTAW constraint in 3D-ProWiz DRAM. This allows 3D-ProWiz to support significantly higher bandwidth than other architectures. To utilize this bandwidth, the memory-to-core interface should support at least a two stage deep pipeline for memory requests with average issue rate of two requests per 16 ns (tTAW for 3D-ProWiz is 16 ns).

This organization enables a 3D-ProWiz module to achieve a peak data rate of 512 x 4 bits/16 ns (2 cachelines/rank/16 ns) assuming a 256-bit cacheline, if the memory controller is designed to send requests to all four ranks in parallel. This is equal to a 128 Gbps peak bandwidth at 1GHz clock rate. This bandwidth analysis assumes close page policy. But, for an open page policy and relatively high row-buffer hit rate, a 3D-ProWiz module can be reasonably assumed to deliver a peak data rate of 512 x 4 bits/2 ns (Burst Length = 2 ns), which is equal to 1,024 Gbps peak bandwidth. A conventional electrical bus based interface of the DDRx family [16], [33] cannot support such a high bandwidth due to pin-bandwidth limitations. To address this issue, the hybrid memory cube from Micron proposes the use of high speed serial links at the interface [10]. The high speed link in HMC consists of several differential lanes as the fundamental building blocks. Each differential lane is claimed to achieve the maximum data transfer rate of 10 Gbps. Thus, 3D-ProWiz would require about 103 such differential lanes to achieve a 1,024 Gbps data transfer rate across the interface. This is a prohibitively large number of lanes that would cause serious packaging issues due to pin-limitations.

Alternatively, several recent works on DRAM architectures have proposed dense wavelength division multiplexed (DWDM) photonic interfaces to achieve higher bandwidths [23], [28]. A DWDM optical fiber can carry approximately 64 wavelengths, which creates 64 channels on a single fiber [29]. A typical DWDM fiber link consists of several components such as ring modulators, photonic waveguides, SerDes (serialization/deserialization) components, and photo detectors, which work together in sync to achieve high speed and high bandwidth data transfers [29], [30]. The resulting bandwidth for a DWDM fiber link depends on the bandwidth of the slowest individual component. In recent years, innovations in Si-photonics technology have enabled on-chip Si waveguides, ring modulators, and ring detectors to function at 10-20 Gbps data rate [31]. Also, advancements in CMOS technology have enabled a single lane SerDes to operate at 25 Gbps data rate [32]. Thus, single wavelength channels within fiber links can today operate at 10 Gbps data rate. In this study, we conservatively operate single wavelength channels within fiber links at 5 Gbps, which corresponds to a 320 Gbps bandwidth per DWDM fiber. Consequently, the bandwidth requirement of 3D-ProWiz can be fulfilled by just 4 such DWDM fibers (~1,280 Gbps), which is easily achievable well within the pin-constraints. Therefore, we propose utilizing such a high bandwidth photonic interface for 3D-ProWiz.

The photonic interface in 3D-ProWiz is comprised of two links (as shown in Fig. 1): one for reads and the other for writes. Each link consists of four unidirectional DWDM fibers. Each DWDM fiber in read and write links supports 64 wavelengths, making the read and write bus to be 256-bits wide each. The photonic interface also uses one additional link consisting of a single DWDM fiber for transmitting address and control signals. The address/control fiber supports a total of 40 wavelengths, with 32 wavelengths for addresses and eight wavelengths for control signaling.

6.2 Design and Functioning of Logic Die

Fig. 11 shows the functional block diagram of the logic die for 3D-ProWiz. The logic die is functionally divided into two parts: photonic and electrical. The photonic part of the logic die performs all of the optical to electrical (O-to-E) and electrical to optical (E-to-O) conversions; and optically interfaces with the memory controller on the processor chip. As shown in the figure, the photonic portion of the logic die consists of on-chip Si waveguides (Si WGs), photonic couplers, and photonic stops. The electrical part of the logic die consists of address/control decoder logic, TSV drivers, read/write buffers, and the control and power delivery network. It interfaces with the DRAM cell array through TSV...
buses. The functionality and role of all of these components on the logic die is discussed next.

For each transaction, firstly the incoming bit stream (originating at the processor side memory controller) from the photonic address/control bus is coupled to the on-chip Si waveguides by couplers. These photonic couplers are primarily responsible for realizing a low loss coupling between on-chip Si waveguides and off-chip DWDM fibers. Next, the bit stream is passed through a photonic stop, where the constituent ring detectors convert the photonic bit stream into an electrical bit stream. The serialized electrical bit stream is then de-serialized before it electrically drives the address/control bus (AB). The signals of this AB are decoded before they are used to drive an appropriate section of one of the TSV buses. The decoded address/control signals activate an appropriate bank to serve the subsequent read or write request. For a write request, the data is written to the requested bank through the TSV bus section.

6.3 Modeling of Interfaces and Energy-Efficiency Analysis

We modeled our proposed photonic interface using the DSENT [25] tool. The timing, energy, and power values for the interface were extracted from DSENT [25], and are given in Tables 4 and 5. In Table 4, the static power for modulators and detectors represents thermal trimming power, whereas it represents leakage power for the rest of the components. We also modeled conventional electrical interfaces such as DDR3 [16], LPDDR3 [33], Wide-I/O [17] and differential interface [34] using CACTI-IO [24]. The configuration parameters used to model the electrical interfaces are given in Table 5. We obtained dynamic energy and static power values of all electrical interfaces from CACTI-IO based simulations, which are given in Table 5. We used the timing, energy and leakage power values given in Tables 4 and 5 to model DDR3, LPDDR3, differential, Wide-I/O and photonic interfaces in DRAMSim2 [26]. We used the timing, energy and leakage power values given in Table 1 to model the 3D-ProWiz core in DRAMSim2.

We integrated the 3D-ProWiz core model with interface models and simulated the following five 3D-ProWiz DRAM subsystems: (1) 3D-ProWiz core with DDR3 interface, (2) 3D-ProWiz core with LPDDR3 interface, (3) 3D-ProWiz core with differential interface, (4) 3D-ProWiz core with Wide-I/O interface, and (5) 3D-ProWiz core with photonic interface. We performed trace-driven simulation analysis for PARSEC benchmarks using DRAMSim2 models of all five aforementioned DRAM subsystems. From DRAMSim2, we obtained energy-per-byte values consumed by the interfaces. In this section, we concentrate on investigating only the interfaces, so we do not report the energy-per-byte values consumed by the 3D-ProWiz core.

For better understanding of the results of these simulations, first consider Fig. 12, which shows a schematic of how a 3D-ProWiz DRAM die-stack can use different type of electrical interfaces to connect to a processor. Fig. 12a shows how the processor can be connected to an off-chip package of 3D-ProWiz die-stack using DDR3, LPDDR3, differential, Wide-I/O and photonic interfaces. The individual dies of the DRAM die-stack are connected to the logic die using TSVs. The logic die in turn is connected to the package substrate using TSVs. The TSVs used for inter-die connections across the die-stack are global or intermediate level TSVs [20]. The 3D-ProWiz package, as shown in Fig. 12, is bonded to the PCB using

### Table 4
Dynamic Energy, Static Power, Losses, and Delay for Photonic Interface Components [23], [25]

<table>
<thead>
<tr>
<th>Component</th>
<th>Dynamic Energy</th>
<th>Static Power</th>
<th>Losses (dB)</th>
<th>Delay (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modulator</td>
<td>47 fJ/bit</td>
<td>250 μW/ring</td>
<td>1</td>
<td>0.5</td>
</tr>
<tr>
<td>Detector</td>
<td>44 fJ/bit</td>
<td>250 μW/ring</td>
<td>1.2</td>
<td>0.5</td>
</tr>
<tr>
<td>Serializer</td>
<td>950 fJ</td>
<td>1.2 mW</td>
<td>-</td>
<td>0.6</td>
</tr>
<tr>
<td>De-serializer</td>
<td>870 fJ</td>
<td>1 mW</td>
<td>-</td>
<td>0.6</td>
</tr>
<tr>
<td><strong>Average Laser Power (mW)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Read/Write Laser Power</td>
<td></td>
<td></td>
<td></td>
<td>131 mW</td>
</tr>
<tr>
<td>Address/Ctrl Laser Power</td>
<td></td>
<td></td>
<td></td>
<td>41 mW</td>
</tr>
</tbody>
</table>

### Table 5
Modeling Parameters for Interfaces

<table>
<thead>
<tr>
<th>Interface Type</th>
<th>DDR3</th>
<th>LP-DDR3</th>
<th>Differential</th>
<th>Wide-I/O</th>
<th>Photonic</th>
</tr>
</thead>
<tbody>
<tr>
<td>#DQ pins/As</td>
<td>64</td>
<td>32</td>
<td>32</td>
<td>128</td>
<td>256</td>
</tr>
<tr>
<td>#DQS pins/As</td>
<td>8</td>
<td>4</td>
<td>4</td>
<td>16</td>
<td>-</td>
</tr>
<tr>
<td>#CA pins/As</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
</tr>
<tr>
<td>Frequency</td>
<td>1 GHz</td>
<td>1 GHz</td>
<td>1 GHz</td>
<td>800 MHz</td>
<td>1 GHz</td>
</tr>
<tr>
<td>AF DQ</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>AF CA</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Energy/256b (nJ)</td>
<td>12.78</td>
<td>7.67</td>
<td>7.43</td>
<td>2.12</td>
<td>0.25</td>
</tr>
<tr>
<td><strong>Static Power (mW)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock</td>
<td>60.75</td>
<td>47.25</td>
<td>47.25</td>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td>PHY</td>
<td>30</td>
<td>47.25</td>
<td>47.25</td>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td>Termination &amp; Bias</td>
<td>2,107.8</td>
<td>1,149.6</td>
<td>48.8</td>
<td>2.3</td>
<td>-</td>
</tr>
<tr>
<td><strong>Total static power of photonic interface</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>455</td>
</tr>
</tbody>
</table>

(AF=Activity Factor, λ=wavelength).
package level TSVs and package ballouts [20]. Similarly, the processor package is bonded to the PCB using package level TSVs and package ballouts.

The interface bus traces are printed on the PCB, which are used to connect the memory package with the processor package through package ballouts, as shown in the figure. Typically, the distance between the memory package and processor package on today’s motherboards/PCBs can be up to 10 cm. The interface bus traces printed on the PCB are similar to standard transmission lines in case of DDR3 and LPDDR3 interfaces, whereas, in case of differential interface, they are similar to low-swing differentially coupled transmission lines. In contrast, the JEDEC standardized Wide-I/O interface is made of TSVs and is used to bond connect two or more devices together to be stacked upon one another. As shown in Fig. 12b, the 3D-ProWiz die-stack can be stacked on the processor die through Wide-I/O TSVs. Due to the TSV-based low-power design of Wide-I/O interface, it is not suitable for connecting the processor to an off-chip memory. The photonic interface in the 3D-ProWiz die-stack can connect to a processor using DWDM fibers through on-chip edge couplers, as shown in Fig. 1.

Fig. 13 shows energy-per-byte values for various interfaces used with the 3D-ProWiz core across the PARSEC benchmarks. It can be observed that the photonic interface consumes about 82 percent less energy-per-byte over all other off-chip interfaces. More specifically, the photonic interface consumes about 88.6, 79.5, and 66.6 percent less energy-per-byte on average over DDR3, differential, and LPDDR3 interfaces respectively. The photonic interface has the shortest burst length (2 cycles) and largest bus width, which results in the highest throughput for the photonic bus. Moreover, as shown in Table 5, the photonic interface has the smallest values of per access dynamic energy and static power, which results in the smallest value of average power. The combined effect of these energy and throughput benefits renders the least energy-per-byte value for the photonic interface among the off-chip interfaces.

However, as shown in Table 5, the Wide-I/O interface has the least static power consumption among all the interfaces. Also, the width of the Wide-I/O interface is comparable to the width of the photonic interface. So, for the Wide-I/O interface, the combined effect of low static power and comparable interface width results in 16.7 percent less energy-per-byte value on average over the photonic interface.

It can be concluded from these results that in case of an off-chip memory, the photonic interface results in the best energy-efficiency over all other interfaces, whereas, if the DRAM is stacked on the processor chip in a single package, Wide-I/O interface proves to be a more promising (energy-efficient) option.

7 SIMULATION RESULTS
7.1 Simulation Setup
We performed trace-driven simulation analysis to compare 3D-ProWiz with other DRAM architectures. Memory access traces for the PARSEC benchmark suite [27] were extracted from detailed cycle-accurate simulations using gem5 [35]. We considered 12 different applications from the PARSEC suite: Blackscholes, Bodytrack, Canneal, Dedup, Facesim, Ferret, Fluidanimate, Freqmine, Streamcluster, Swaptions, Vips, and x264. We ran each PARSEC benchmark for a “warm-up” period of one billion instructions and captured memory access traces from the subsequent one billion instructions extracted. These memory traces were then provided as inputs to the DRAM simulator DRAMSim2 [26], which we used to model 3D-ProWiz and other DRAM architectures. Table 6 gives the configuration of Gem5 that was used for this study. We chose direct mapped cache associativity because of its simplicity and low cost implementation. The use of N-way set associative cache would change the memory access pattern, and hence it would change the behavior of the DRAM subsystem. But, the effect of different memory access patterns on the system behavior is captured by the different kinds of applications from the PARSEC benchmark suite used in this study. For this reason and for the sake of brevity we do not include the evaluation results for different cache associativities in this paper.

We used the timing, energy and static power values given in Table 1 to characterize the various DRAM architecture in DRAMSim2. We modeled memory interfaces using the method discussed in Section 6.3. Table 7 shows the memory configurations used in DRAMSim2 for the comparison across different DRAM architectures. As discussed in Section 4, the interface used with 3DSams in [9] closely resembles the low power DDR3 interface LPDDR3. Therefore, for this study, we use LPDDR3 interface with the 3DSams DRAM. As shown in Table 7, we use DDR3, differential and photonic interfaces with the DDR3, HMC and 3D-ProWiz DRAMs respectively. An RBRR scheduling scheme, an open page policy and rank:
row:col:bank address mapping scheme were used for all simulations. Average latency, total power consumption, and energy-delay product values for the memory subsystem were obtained from DRAMSim2. The results of simulations with PARSEC benchmarks are discussed in the following section.

### 7.2 Simulation Results for PARSEC Benchmarks

This section presents the average latency, power, and energy-delay product values for the 3D DRAM designs shown in Table 7 obtained for PARSEC benchmarks. Fig. 14 shows power consumption values for the various DRAM architectures across the PARSEC benchmarks. It can be observed that 3D-ProWiz consumes about 52 percent less power on average over all the other DRAM architectures. More specifically, 3D-ProWiz consumes about 75.3, 23.4 and 58.3 percent less power on average over DDR3, 3DSAMS and HMC respectively. 3DSPDRAM consumes about 72.3 percent less power on average over 3D-ProWiz. In fact, 3DSPDRAM consumes the least amount of power across all the DRAMs. The reason behind it is the single-subarray-architecture (SSA) architecture in 3DSPDRAM, which yields the smallest value of activation-precharge energy resulting in the lowest power consumption. The reason for the lower power consumption in 3D-ProWiz compared to other DRAMs is its smaller values of per-access energy, the effect of which cumulates over time to minimize average power consumption.

Fig. 15 shows the average latency values for different DRAM designs across the PARSEC benchmarks. The average latency was calculated by dividing the total latency by total number of transactions. 3D-ProWiz demonstrates about 41.9 percent less average latency over all the other 3D DRAM architectures. More specifically, 3D-ProWiz demonstrates 35.1, 31.3, 61.5 and 22.9 percent lower average latency values over DDR3, 3DSAMS, 3DSPDRAM and HMC respectively. As discussed in Section 2 and in [15], the fine-grained rank-level 3D partitioning of the data array in HMC better utilizes potential TSV bandwidth compared to the coarse-grained rank-level partitioning used in 3DSPDRAM and 3DSAMS. Due to this reason, HMC has an edge over 3DSPDRAM and 3DSAMS, which translates into a performance edge for HMC over 3DSPDRAM and 3DSAMS. The reason behind the better performance of 3D-ProWiz over other DRAM designs is the reduced RC loading of the access path in 3D-ProWiz, which is a result of the smaller subarrays and elimination of global lines in the architecture. As implied from the discussion given in Section 4, the increased serialization delay of the SSA architecture of 3DSPDRAM results in larger average latency for 3DSPDRAM compared to other DRAMs with photonic interfaces.

Fig. 16 shows the energy-delay product values for different DRAM designs across the PARSEC benchmarks. EDP values were calculated by multiplying the average-energy with average latency for memory accesses. Average-energy in each benchmark was calculated by dividing the total energy by total number of transactions. 3D-ProWiz yields an 80.6 percent lower EDP value on average over all the other 3D DRAM architectures. More specifically, 3D-ProWiz yields 89.7, 64.4, 75.1 and 75.6 percent less EDP values on average over DDR3, 3DSAMS, 3DSPDRAM and HMC respectively. These improvements in EDP for 3D-ProWiz follow directly from the power and latency improvements that were discussed earlier.

In summary, the 3D vertical routing of the internal memory bus using TSVs at subarray-level granularity and fanout

---

### TABLE 6

<table>
<thead>
<tr>
<th>#Cores</th>
<th>4 ARM</th>
<th>L2 Coherence</th>
<th>MOESI</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1 Cache</td>
<td>16 KB</td>
<td>Frequency</td>
<td>5 GHz</td>
</tr>
<tr>
<td>L1 D Cache</td>
<td>16 KB</td>
<td>Issue Policy of cores</td>
<td>In-order</td>
</tr>
<tr>
<td>L2 Cache</td>
<td>128 KB</td>
<td># Memory Controllers</td>
<td>1</td>
</tr>
<tr>
<td>Cache Associativity</td>
<td>Direct Mapped</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### TABLE 7

<table>
<thead>
<tr>
<th>DRAMSim2 Simulation Configurations</th>
</tr>
</thead>
<tbody>
<tr>
<td>3D-ProWiz</td>
</tr>
<tr>
<td>HMC</td>
</tr>
<tr>
<td>3DSPDRAM</td>
</tr>
<tr>
<td>3DSams</td>
</tr>
<tr>
<td>DDR3</td>
</tr>
</tbody>
</table>
buffers enable 3D-ProWiz to use smaller dimension subarrays. This in turn reduces the random access latency and activation-precharge energy of 3D-ProWiz DRAM over other DRAM designs. Consequently, 3D-ProWiz yields on average 52, 41.9 and 80.6 percent improvements in power consumption, latency and energy-delay product respectively over other DRAM architectures. 3D-ProWiz DRAM has about 9.16 mm$^2$ (41.7 percent) more die area than the average die area of other DRAMs, which increases its relative cost. Nonetheless, the significant improvements in access latency, power, and energy-efficiency make 3D-ProWiz a promising architecture candidate for future 3D DRAMs.

8 Conclusions

This paper introduced 3D-ProWiz, a novel high bandwidth and low-latency 3D DRAM architecture. 3D-ProWiz integrates sub-bank level 3D partitioning of the data array to enable fine-grained activation and greater memory parallelism than other 3D DRAM architectures. The 3D vertical routing of the internal memory bus using TSVs at subarray-level granularity and fanout buffers enable 3D-ProWiz to use smaller dimension subarrays without significant area overhead. This in turn reduces the random access latency and activation-precharge energy. Consequently, 3D-ProWiz yields on average 52, 41.9 and 80.6 percent improvements in power consumption, latency and energy-delay product respectively over other DRAM architectures.

Detailed sensitivity analysis of the tTAW constraint in this work established that it is very important to design a robust PDN, which is less prone to noise and which has more relaxed tTAW constraint, for a 3D DRAM subsystem with relatively small row cycle time and large bank count. We also showed in this work that, in case of an off-chip memory, the photonic interface renders the best energy-efficiency over all other interfaces, whereas, if the memory is embedded with the processor chip in a single package, the Wide-I/O interface proves to be more promising and energy-efficient option.

The significant improvements demonstrated by 3D-ProWiz position it as a promising architecture for future DRAMs. The performance of the 3D-ProWiz memory system can be further improved by using intelligent scheduling schemes and novel memory controller designs so that the greater parallelism of 3D-ProWiz architecture can be better exploited. Moreover, the capacity of the 3D-ProWiz DRAM module can be greatly scaled by using intelligent arbitration techniques for the photonic bus. Thus, with potential opportunities for further improvements, the 3D-ProWiz architecture can become an even more promising solution for future DRAM implementations.

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References


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