CV-Ishan G Thakkar

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1 Personal Information

1.1 Contact Information

Dr. Ishan G Thakkar
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1.2 Key Highlights

- Research funded by NSF, DOE; Principal effort amount $756,054 (total $3,093,554).
- In-kind research grant contributions, total amount of $100,000+.
- 6 Best Paper Awards and Nominations from peer-reviewed journals and conferences.
- Outstanding Reviewer Award from IEEE/ACM CODES+ISSS at ESWEEK 2022.
- 4 Best Poster Awards to my students at research symposia.
- Graduated 3 Ph.D. and 2 M.S. Thesis students.
- 55+ peer-reviewed publications in top journals and premier conferences.
- 10+ chaired positions in organizing committees of IEEE/ACM conferences/workshops.
- 30+ technical program committees of IEEE/ACM conferences.

1.3 Professional Experience

2018 – Present *Assistant Professor*
Department of Electrical and Computer Engineering,
University of Kentucky, Lexington, KY, USA
From August 01, 2018 to Present
Note: The tenure clock was delayed by 2 years due to COVID-19 and a life-changing family health event, marking the effective start of the clock in July 2020.

2013 – 2018	*Graduate Research and Teaching Assistant* Embedded Systems and High-Performance Computing (EPiC) Lab, Colorado State University, Fort Collins, CO, USA From August 2013 to May 2018.
2012 – 2013	*Graduate Research Assistant* Optoelectronics Research Group, Colorado State University, Fort Collins, CO, USA From January 2012 to May 2013
Spring/Fall 2011	*Graduate Teaching Assistant* Department of Electrical and Computer Engineering, Colorado State University, Fort Collins, CO, USA
Summer 2011	*Research Intern* Microwave Systems Laboratory, Colorado State University, Fort Collins, CO, USA
2009-2010	*Ad-hoc Lecturer* Department of Computer Engineering, Venus International College of Technology, Gujarat, India From June 2009 to July 2010
2009	*Project Intern* Peach Technovations Pvt. Ltd., Gandhinagar, Gujarat, India From January 2009 to June 2009

1.4 Education

2013-2018	*Ph.D. in Electrical Engineering* Colorado State University, Fort Collins, CO, USA Dissertation: Design and Optimization of Emerging Interconnection and Memory Subsystems for Future Manycore Architectures Advisor: Sudeep Pasricha
2010-2013	*M.S. in Electrical Engineering* Colorado State University, Fort Collins, CO, USA Thesis: A plastic total internal reflection-based photoluminescence device for enzymatic biosensors Advisor: Kevin L. Lear
2005-2009	*B.E. in Electronics and Communication Engineering* L.D. College of Engineering, Ahmedabad, Gujarat, India
2003-2005	*High School, Gujarat State Higher Secondary Board* Sheth Chimanlal Nagindas Vidyavihar, Ambavadi, Ahmedabad, Gujarat, India

1.5 Awards and Honors

[AH8] – ***Research Recognition Awards and Travel Grants to Students (Multiple).*** 2023 and 2022. My students have received multiple Best Poster Awards and Travel Grants at various workshops, symposia, and conferences. Specific details are included in Section 3.11. These awards include 4 Best Poster Awards in Various Categories at the 2022 and 2023 Annual Research Symposia of the ECE Department of UKY

[AH7] – *Outstanding Reviewer Award.* 2022. IEEE/ACM Embedded Systems Week (ESWEEK) - the International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS).

[AH6] – *Best Paper Award Finalist Selection.* 2021. IEEE Computer Society Annual Symposium on VLSI (ISVLSI), "ATRIA: A Bit-Parallel Stochastic Arithmetic Based Accelerator for In-DRAM CNN Processing," July, Virtual Event.

[AH5] – *Best Paper Award*. 2021. ACM Great Lakes Symposium on VLSI (GLSVLSI), "Characterization and Mitigation of Electromigration Effects in TSV-Based Power Delivery Network Enabled 3D-Stacked DRAMs," June, Virtual Event. (with an undergraduate student, Bobby Bose)

[AH4] – *Best Paper Award Honorary Selection.* 2020. ACM Great Lakes Symposium on VLSI (GLSVLSI), "LORAX: Loss-Aware Approximations for Energy-Efficient Silicon Photonic Networks-on-Chip," September, Virtual Event.

[AH3] – *Best Journal Paper Award Candidate.* 2017. IEEE Transactions on Multi-Scale Computing Systems (TMSCS), "3D-ProWiz: An Energy-Efficient and Optically Interfaced 3D DRAM Architecture with Reduced Data Access Overhead".

[AH2] – *Best Paper Award.* 2016. ACM System Level Interconnect Prediction (SLIP) Workshop, "A Comparative Analysis of Front-End and Back-End Compatible Silicon Photonic On-Chip Interconnects," Austin, Texas, USA.

[AH1] – *Best Paper Award Finalist.* 2016. IEEE International Symposium on Quality Electronic Design (ISQED), "Process Variation Aware Crosstalk Mitigation for DWDM based Photonic NoC Architectures," Santa Clara, California, USA.

1.6 Professional Society Membership

2018-Present	IEEE Member
2018-Present	ACM Member
2016-2018	ACM Student Member
2014-2018	IEEE Student Member

2 Research Activities

2.1 Research Interest Statement

My research broadly focuses on designing and optimizing unconventional (More-than-Moore) architectures and technologies for energy-efficient, reliable, and secure computing, for a wide range of platforms including embedded systems, internet-of-things (IoT), and high-performance computing systems. More specific More-than-Moore technology interests include (1) Silicon photonics; (2) Optical computing; (3) Neuromorphic computing; (4) In-memory computing; (5) Stochastic computing; (6) Monolithic 3D (M3D) integration; (7) Polymer and transparent conductive oxides based photonic devices and sensors. More specific topics of interest include i) design of on-chip and inter-chip networks, ii) memory architecture design, iii) 3D integrated chip design, iv) design with emerging technologies, e.g., silicon photonics, phase change materials, spintronics, v) self-adaptive and cognitive architectures, vi) manycore hardware security, vii) high-speed optical interfaces, viii) resource management techniques, and ix) optoelectronic/photonic sensors and devices.

2.2 Awarded Research Grants and Contracts

[ARG4] – Department of Energy (DOE), Established Program to Stimulate Competitive Research (EPSCoR) Implementation Grant. **Co-Principal Investigator** (PI: Todd Hastings; Other Co-PIs from UKY: Lance Delong, Henry Dietz, Thomas Balk, Paul Rottmann, Douglas Strachan, Ganapathy Murthy, Beth Guiton, William Gannon, Chunli Huang; non-UKY Co-PIs: Benjamin Jungfleisch from the University of Delaware, Stephen Johnson from Transylvania University; Other Collaborators from Lawrence Berkeley National Laboratory, Brookhaven National Laboratory, Oak Ridge National Laboratory, and Argonne National Laboratory). *Light-Matter Interactions in Artificial Spin Lattices*. Oct. 2021 to Sept. 2024, **$2,750,000** (My effort is 15%, **$412,500**). (DE-SC0024346)

[ARG3] – National Science Foundation (NSF), Division of Computer and Network Systems (CNS), Computer Systems Research (CSR). **Principal Investigator** (Co-PI: Todd Hastings). *Supplemental Grant for Access to Semiconductor Fabrication. EAGER: Transforming Optical Neural Network Accelerators with Stochastic Computing*. Oct. 2021 to Sept. 2024, **$43,819**. (NSF CNS-2139167)

[ARG2] – Argonne National Laboratory, User Access Contract with Center for Nanoscale Materials. **Principal Investigator** (Co-PIs: Justin Woods, Jeffrey Todd Hastings). *Silicon Nitride Microring Modulators for High-Performance Photonic Integrated Circuits*. From Dec. 2021, **~$120,000** (estimated in-kind amount near the lower bound**)**

[ARG1] – National Science Foundation (NSF), Division of Computer and Network Systems (CNS), Computer Systems Research (CSR). **Principal Investigator** (Co-PIs: Todd Hastings, Sayed Ahmad Salehi). *EAGER: Transforming Optical Neural Network Accelerators with Stochastic Computing*. Oct. 2021 to Sept. 2023, **$299,735**. (NSF CNS-2139167)

2.3 Pending Research Grants

[PERG4] – Department of Energy (DOE), Office of Science (SC), Advanced Scientific Computing Research (ASCR), Advancements in Artificial Intelligence for Science (DE-FOA-0003264).

Collaborative Proposal. **Principal Investigator**. (Co-PI: Patricia Guerrero-Gonzalez and George Michelogiannakis from Lawrence Berkeley National Laboratory). Pre-application approved in April 2024. Full proposal submitted in May 2024. For 3 years, **$3,720,000** (UKY's share $1,046,932).

[PERG3] - National Science Foundation (NSF), Directorate for Computer and Information Science and Engineering, Enabling Access to the Semiconductor Chip Ecosystem for Design, Fabrication, and Training (Chip Design Hub). **Lead PI** for proposed efforts at the University of Kentucky. *Chip Design Hub: ARIES—An Egalitarian IC Design Hub.* Ohio State University will lead the hub to have five centers. The University of Kentucky (UKY) will partner with the University of Louisville (UofL) Center. The total requested amount for the UofL Center is **$1,200,000** (Subaward to UKY will be $265,000).

[PERG2] – Kentucky EPSCoR Statewide Office. **Principal Investigator**. *KY EPSCoR Matching for Extreme-Scale Tensor Processing with Massively Parallel Electro-Photonic Architectures*. **$100,000**.

[PERG1] – Department of Energy (DOE), EPSCoR-State / National Laboratory Partnerships Program (DE-FOA-0003201). **Principal Investigator**. (Senior Personnel on mentorship roles: Lingda Li, George Michelogiannakis, Henry Dietz, J. Todd Hastings). *Extreme-Scale Tensor Processing with Massively Parallel Electro-Photonic Architectures*. Pre-application approved in Jan. 2024. Full proposal submitted in Feb. 2024. For 4 years, **$997,500**.

2.4 Other Research Contracts and Agreements

[ORCA2] – Mutual Confidentiality Agreement between Advanced Micro Foundry Pte. Ltd. and The University of Kentucky, *research collaboration agreement for integrated silicon-photonic circuits design and fabrication*. It was signed in September 2021, for 3 years.

[ORCA1] – Mutual Confidentiality Agreement between SiEPIC Kits Ltd. and The University of Kentucky, a *research collaboration agreement for the characterization and testing of integrated silicon-photonic devices and circuits*. It was signed in September 2020, for 3 years.

2.5 Note on Publication Categories

After each publication (article/paper/chapter/patent/poster/presentation/talk) listed in different categories below, one of the following code letters is used to indicate the nature of the review process. This code letter is followed by a double asterisk (**) for publications with one of my graduate/undergraduate students at UKY. ***A double asterisk (**) after an author's name indicates that the author is my student at UKY***.

- **W** Full publication reviewed by one or more anonymous referees; involves multiple stages of revisions and rebuttals
- **W--** Full publication reviewed by more than one anonymous referee; rigorous review as in the W category; low acceptance rate (15%-30%); publishing in this category is often harder than publishing in the W category because of the low acceptance rate and as no revisions are allowed
- **X** Full publication reviewed by an editor or by the conference organizing committee ` invited
- **Y** Only abstract is reviewed
- **Z+** Not reviewed at the time of submission/acceptance, but judged by peers, editor or conference committee, etc., afterward

Z Not reviewed

2.6 Research Book Chapters

[BC6] – Ishan Thakkar, *Supreeth Mysore Shivanandamurthy***, Sayed Ahmad Salehi, "Low-Latency, Energy-Efficient In-DRAM CNN Acceleration with Bit-Parallel Unary Computing," Embedded Machine Learning for Cyber-Physical, IoT, and Edge Computing, Springer Nature, 2023. **(X)****

[BC5] – Febin Sunny, Asif Mirza, Ishan Thakkar, Sudeep Pasricha, Mahdi Nikdast, "Improving Energy Efficiency in Silicon Photonic Networks-on-Chip with Approximation Techniques," Silicon Photonics for High-Performance Computing and Beyond, CRC Press/Taylor & Francis Group, 2021. **(X)**

[BC4] – Ishan Thakkar, Sai Vineel Reddy Chittamuru, Varun Bhat, *Sairam Sri Vatsavai***, Sudeep Pasricha, "Securing Silicon Photonic NoCs Against Hardware Attacks", Springer Book on Network-on-Chip Security and Privacy, 2021. **(X)****

[BC3] – Ishan Thakkar, Sai Vineel Reddy Chittamuru, Varun Bhat, *Sairam Sri Vatsavai***, Sudeep Pasricha, "Hardware Security in Emerging Photonic Network-on-Chip Architectures," Silicon Photonics for High-Performance Computing and Beyond, Springer Book on Emerging Computing, June 2020. **(X)****

[BC2] – Ishan Thakkar, Sudeep Pasricha, *Venkata Sai Praneeth Karempudi***, Sai Vineel Reddy Chittamuru, "Exploring Aging Effects in Photonic Interconnects for High-Performance Manycore Architectures," Silicon Photonics for High-Performance Computing and Beyond, CRC Press/Taylor & Francis Group, December 2019. **(X)****

[BC1] - Sudeep Pasricha, Sai Vineel Reddy Chittamuru, Ishan Thakkar, "Enhancing Process Variation Resilience in Photonic NoC Architectures," Photonic Interconnects for Computer Systems – Understanding and Pushing Design Challenges, River Publishers, June 2017. **(X)**

2.7 Archived Papers

[AP1] – *Supreeth Mysore Shivanandamurthy***, Ishan Thakkar, Sayed Ahmad Salehi, "ODIN: A Bit-Parallel Stochastic Arithmetic Based Accelerator for In-Situ Neural Network Processing in Phase Change RAM," arXiv:2103.03953, January 2020.

2.8 Peer-Reviewed Journal Publications (Full-Papers)

[J16] – Salma Afifi, Ishan Thakkar, and Sudeep Pasricha, "ARTEMIS: A Mixed Analog-Stochastic In-DRAM Accelerator for Transformer Neural Networks," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD). 2024. **(Under Revision) (W)**

[J15] – Salma Afifi, Ishan Thakkar, and Sudeep Pasricha, "STAR: A Mixed Analog Stochastic In-DRAM Convolutional Neural Network Accelerator," IEEE Design and Test, 2024. **(Under Revision) (W)**

[J14] – *Venkata Sai Praneeth Karempudi***, *Sairam Sri Vatsavai***, Ishan Thakkar, "HEANA: A Hybrid Time-Amplitude Analog Optical Accelerator with Flexible Dataflows for Energy-Efficient

CNN Inference," ACM Transactions on Design Automation of Electronic Systems (TODAES), 2024. **(First Revision Under Review) (W)****

[J13] – *Venkata Sai Praneeth Karempudi***, *Sairam Sri Vatsavai***, Ishan Thakkar, "A Hybrid Time-Amplitude Analog Photonic Accelerator for General Matrix-Matrix Multiplications," Journal of Applied Physics (JAP), 2024. **(Under Revision) (W)****

[J12] – *Venkata Sai Praneeth Karempudi***, Janibul Bashir, Ishan Thakkar, "An Analysis of Various Design Pathways Towards Multi-Terabit Photonic On-Interposer Interconnects," ACM Journal on Emerging Technologies in Computing Systems (JETC), 2023. **(W)****

[J11] – *Sairam Sri Vatsavai***, Ishan Thakkar, "Photonic Reconfigurable Accelerators for Efficient Inference of CNNs With Mixed-Sized Tensors," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 41, no. 11, 2022. **(W)****

[J10] – Amlan Ganguly, Sergi Abadal, Ishan Thakkar, Natalie Enright Jerger, Marc Riedel, Masoud Babaie, Rajeev Balasubramanian, Abu Sebastian, Sudeep Pasricha, Baris Taskin, "Interconnects for DNA, Quantum, In-Memory and Optical Computing: Insights from a Panel Discussion," IEEE Micro, 2022. **(W)**

[J9] – *Venkata Sai Praneeth Karempudi***, Febin Sunny, Ishan Thakkar, Sai Vineel Reddy Chittamuru, Mahdi Nikdast, Sudeep Pasricha, "Photonic Networks-on-Chip Employing Multilevel Signaling: A Cross-Layer Comparative Study," ACM Journal on Emerging Technologies in Computing Systems (JETC), 2021. **(W)****

[J8] – Febin Sunny, Asif Mirza, Ishan Thakkar, Mahdi Nikdast, Sudeep Pasricha, "ARXON: A Framework for Approximate Communication over Photonic Networks-on-Chip", accepted in IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 2021. **(W)**

[J7] – Sai Vineel Reddy Chittamuru, Ishan Thakkar, Sudeep Pasricha, *Sairam Sri Vatsavai***, Varun Bhat, "Exploiting Process Variations to Secure Photonic NoC Architectures from Snooping Attacks," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2020. **(W)****

[J6] – Sai Vineel Reddy Chittamuru, Ishan Thakkar, Sudeep Pasricha, "LIBRA: Thermal and Process Variation Aware Reliability Management in Photonic Networks-on-Chip," accepted for publication in IEEE Transactions on Multi-Scale Computing Systems (TMSCS), June 2018. **(W)**

[J5] – Ishan Thakkar, Sudeep Pasricha, "DyPhase: A Dynamic Phase Change Memory Architecture with Symmetric Write Latency and Restorable Endurance," IEEE Transactions on Computer Aided Design (TCAD), vol. 37, no. 9, pp. 1760-1773, September 2018. **(W)**

[J4] – Sai Vineel Reddy Chittamuru, Ishan Thakkar, Sudeep Pasricha, "HYDRA: Heterodyne Crosstalk Mitigation with Double Microring Resonators and Data Encoding for Photonic NoCs," IEEE Transactions on Very Large-Scale Integration (TVLSI), vol. 26, no. 1, pp. 168-181, January 2018. **(W)**

[J3] – Ishan Thakkar, Sudeep Pasricha, "3D-ProWiz: An Energy-Efficient and Optically-Interfaced 3D DRAM Architecture with Reduced Data Access Overhead," IEEE Transactions on Multi-Scale

Computing Systems (TMSCS), vol. 1, no. 3, pp. 168-184, September 2015. **(Best Paper Candidate) (W)**

[J2] – Ishan Thakkar, Sudeep Pasricha, "3D-WiRED: A Novel WIDE I/O DRAM with Energy-Efficient 3-D Bank Organization," IEEE Design & Test, vol. 32, no. 4, pp. 71-80, August 2015. **(W)**

[J1] – Ishan Thakkar, Kevin L Lear, Jonathan Vickers, Brian Heinze, and Kenneth Reardon, "A plastic total internal reflection photoluminescence device for enzymatic biosensing," Lab Chip, vol. 13, no. 34, pp. 4775-4783, December 2013. **(W)**

2.9 Peer-Reviewed Conference Publications (Full-Papers; approximately 15-30% acceptance rate)

[C41] – *Oluwaseun Adewunmi Alo***, *Sairam Sri Vatsavai***, Ishan Thakkar, "Scaling Analog Photonic Accelerators for Byte-Size, Integer General Matrix Multiply (GEMM) Kernels," IEEE Computer Society Annual Symposium on VLSI (ISVLSI), July 2024**. (W⁻⁻)****

[C40] – *Venkata Sai Praneeth Karempudi***, *Sairam Sri Vatsavai***, Ishan Thakkar, Justin Woods, Jeffrey Todd Hastings, "A Low-Dissipation and Scalable GEMM Accelerator with Silicon Nitride Photonics," IEEE International Symposium on Quality Electronic Design (ISQED'24), April 2024. **(W⁻)****

[C39] – *Sairam Sri Vatsavai***, *Venkata Sai Praneeth Karempudi***, and Ishan Thakkar, "A Comparative Analysis of Microrings Based Incoherent Photonic GEMM Accelerators," IEEE International Symposium on Quality Electronic Design (ISQED'24), April 2024. **(W⁻⁻)****

[C38] – *Sairam Sri Vatsavai***, *Venkata Sai Praneeth Karempudi***, and Ishan Thakkar, "An Electro-Photonic Unary Multiply-Accumulate (MAC) Circuit," to appear at IEEE/APS/OPTICA Conference on Lasers and Electro-Optics (CLEO), May 2024. **(W⁻⁻)****

[C37] – *Venkata Sai Praneeth Karempudi***, Ishan Thakkar, Justin Woods, and Jeffrey Todd Hastings, "A Hybrid Time-Amplitude Analog MAC Circuit with Silicon Nitride Electro-Photonics," to appear at IEEE/APS/OPTICA Conference on Lasers and Electro-Optics (CLEO), May 2024. **(W⁻)****

[C36] – Henry Dietz, Hironori Kasahara, Movahhed Sadeghi, Ishan Thakkar, "Evolution of Parallel Architecture Targets," the 36th International Workshop on Languages and Compilers for Parallel Computing (LCPC), October 2023. **(W⁻⁻)**

[C35] – Ishan Thakkar, *Sairam Sri Vatsavai***, *Venkata Sai Praneeth Karempudi***, "High-Speed and Energy-Efficient Non-Binary Computing with Polymorphic Electro-Optic Circuits and Architectures," ACM Great Lakes Symposium on VLSI (GLSVLSI), June 2023. **(W⁻⁻)****

[C34] – *Sairam Sri Vatsavai***, Ishan Thakkar, "A Bit-Parallel Deterministic Stochastic Multiplier," IEEE International Symposium on Quality Electronic Design (ISQED'23), April 2023. **(W⁻⁻)****

[C33] – *Supreeth Mysore Shivanandamurthy***, *Sairam Sri Vatsavai***, Ishan Thakkar, Sayed Ahmad Salehi, "AGNI: In-Situ, Iso-Latency Stochastic-to-Binary Number Conversion for In-DRAM Deep

Learning," IEEE International Symposium on Quality Electronic Design (ISQED'23), April 2023. **(W⁻)****

[C32] – *Venkata Sai Praneeth Karempudi***, *Sairam Sri Vatsavai***, Ishan Thakkar, Jeffrey Todd Hastings, "A Polymorphic Electro-Optic Logic Gate for High-Speed Reconfigurable Computing Circuits," IEEE International Symposium on Quality Electronic Design (ISQED'23), April 2023. **(W⁻)****

[C31] – *Sairam Sri Vatsavai***, *Venkata Sai Praneeth Karempudi***, Ishan Thakkar, "An Optical XNOR-Bitcount Based Accelerator for Efficient Inference of Binary Neural Networks," IEEE International Symposium on Quality Electronic Design (ISQED'23), April 2023. **(W⁻)****

[C30] – *Sairam Sri Vatsavai***, *Venkata Sai Praneeth Karempudi***, Ishan Thakkar, Jeffrey Todd Hastings, Sayed Ahmad Salehi, "SCONNA: A Stochastic Computing Based Optical Accelerator for Ultra-Fast, Energy-Efficient Inference of Integer-Quantized CNNs," IEEE International Parallel & Distributed Processing Symposium (IPDPS), May 2023. **(W⁻)****

[C29] – *Venkata Sai Praneeth Karempudi***, Ishan Thakkar, Jeffrey Todd Hastings, "A Silicon Nitride Microring Based High-Speed, Tuning-Efficient, Electro-Refractive Modulator," IEEE International Symposium on Smart Electronic Systems (iSES), Warangal, India, December 2022. **(W⁻)****

[C28] – *Sairam Sri Vatsavai***, Ishan Thakkar, "Photonic Reconfigurable Accelerators for Efficient Inference of CNNs With Mixed-Sized Tensors," IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), October 2022. **(W⁻)****

[C27] – *Venkata Sai Praneeth Karempudi***, Shreyan Datta, Ishan Thakkar, "Design Exploration and Scalability Analysis of a CMOS-Integrated, Polymorphic, Nanophotonic Arithmetic-Logic Unit," ACM Conference on Embedded Networked Sensor Systems (SenSys) 2021. **(W⁻)****

[C26] – *Supreeth Mysore Shivanandamurthy***, Ishan Thakkar, Sayed Ahmad Salehi, "ATRIA: A Bit-Parallel Stochastic Arithmetic Based Accelerator for In-DRAM CNN Processing," IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2021. **(Best Paper Award Nominee)** **(W⁻)****

[C25] – *Bobby Bose***, Ishan Thakkar, "Characterization and Mitigation of Electromigration Effects in TSV-Based Power Delivery Network Enabled 3D-Stacked DRAMs," ACM Great Lakes Symposium on VLSI (GLSVLSI), June 2021. **(Best Paper Award)** **(W⁻)****

[C24] – *Sairam Sri Vatsavai***, Ishan Thakkar, "Silicon Photonic Microring Based Chip-Scale Accelerator for Delayed Feedback Reservoir Computing," IEEE 34th International Conference on VLSI Design & 20th International Conference on Embedded Systems (VLSID 2021), February, 2021. **(W⁻)****

[C23] – *Chao-Hsuan Huang***, Ishan Thakkar, "Mitigating the Latency-Area Tradeoffs for DRAM Design with Coarse-Grained Monolithic 3D (M3D) Integration," IEEE International Conference on Computer Design (ICCD), October, 2020. **(W⁻)****

[C22] – *Sairam Sri Vatsavai***, *Venkata Sai Praneeth Karempudi***, Ishan Thakkar, "PROTEUS: Rule-Based Self-Adaptation in Photonic NoCs for Loss-Aware Co-Management of Laser Power and Performance," IEEE/ACM International Symposium on Networks-on-Chip (NOCS), September, 2020. **(W⁻)****

[C21] – *Febin Sunny*, Asif Mirza, Ishan Thakkar, Sudeep Pasricha, Mahdi Nikdast, "LORAX: Loss-Aware Approximations for Energy-Efficient Silicon Photonic Networks-on-Chip," ACM Great Lakes Symposium on VLSI (GLSVLSI), May, 2020. **(Best Paper Award Honorary Selection) (W⁻)**

[C20] – *Venkata Sai Praneeth Karempudi***, *Sairam Sri Vatsavai***, Ishan Thakkar, "Redesigning Photonic Interconnects with Silicon-on-Sapphire Device Platform for Ultra-Low-Energy On-Chip Communication," ACM Great Lakes Symposium on VLSI (GLSVLSI), May, 2020. **(W⁻)****

[C19] – *Venkata Sai Praneeth Karempudi***, Ishan Thakkar, "Mitigating Inter-Channel Crosstalk Non-Uniformity in Microring Filter Arrays of Wavelength-Multiplexed Photonic NoCs," ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), New York, NY, USA, October 2019. **(W⁻)****

[C18] – *Supreeth Mysore Shivanandamurthy***, Ishan Thakkar, Sayed Ahmad Salehi, "A Scalable Stochastic Number Generator for Phase Change Memory-Based In-Memory Stochastic Processing," ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), New York, NY, USA, October 2019. **(W⁻)****

[C17] - *Chao-Hsuan Huang**, Ishan Thakkar, "Mitigating Write Disturbance in Phase Change Memory," ACM/IEEE International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), New York, NY, USA, October 2019. **(W⁻)****

[C16] - Ishan Thakkar, Sai Vineel Reddy Chittamuru, Sudeep Pasricha, "Mitigating the Energy Impacts of VBTI Aging in Photonic Networks-on-Chip Architectures with Multilevel Signaling," IEEE Workshop on Energy-efficient Networks of Computers (E2NC): from the Chip to the Cloud, Pittsburgh, PA, USA, October 2018. **(W⁻)**

[C15] - Sudeep Pasricha, Sai Vineel Reddy Chittamuru, Ishan Thakkar, Varun Bhat, "Securing Photonic NoCs from Hardware Trojans," IEEE/ACM International Symposium on Networks-on-Chip (NOCS), Torino, Italy, October 2018. **(W⁻)**

[C14] - Sudeep Pasricha, Sai Vineel Reddy Chittamuru, Ishan Thakkar, "Cross-Layer Thermal Reliability Management in Silicon Photonic Networks-on-Chip," ACM Great Lakes Symposium on VLSI (GLSVLSI), Chicago, IL, USA, May 2018. **(W⁻)**

[C13] - Sai Vineel Reddy Chittamuru, Ishan Thakkar, Varun Bhat, Sudeep Pasricha, "SOTERIA: Exploiting Process Variations to Enhance Hardware Security with Photonic NoC Architectures," IEEE/ACM Design Automation Conference (DAC), San Francisco, CA, USA, June 2018. (acceptance rate: 168/691 = 24.3%) **(W⁻)**

[C12] - Ishan Thakkar, Sai Vineel Reddy Chittamuru, Sudeep Pasricha, "Improving the Reliability and Energy-Efficiency of High-Bandwidth Photonic NoC Architectures with Multilevel Signaling,"

IEEE/ACM International Symposium on Networks-on-Chip (NOCS), Seoul, South Korea, October 2017. (acceptance rate: 14/44 = 31.8%) **(W--)**

[C11] - Sai Vineel Reddy Chittamuru, Ishan Thakkar, Sudeep Pasricha, "Analyzing Voltage Bias and Temperature Induced Aging Effects in Photonic Interconnects for Manycore Computing," ACM System Level Interconnect Prediction Workshop (SLIP), Austin, TX, USA, June 2017. **(W--)**

[C10] - Ishan Thakkar, Sudeep Pasricha, "DyPhase: A Dynamic Phase Change Memory Architecture with Symmetric Write Latency," IEEE International Conference on VLSI Design (VLSID), Hyderabad, India, January 2017. (acceptance rate: 71/292 = 24.3%) **(W--)**

[C9] - Ishan Thakkar, Sai Vineel Reddy Chittamuru, Sudeep Pasricha, "Mitigation of Homodyne Crosstalk Noise in Silicon Photonic NoC Architectures with Tunable Decoupling," ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), Pittsburgh, PA, USA, October 2016. (acceptance rate: 21/80 = 26.3%) **(W--)**

[C8] - Ishan Thakkar, Sai Vineel Reddy Chittamuru, Sudeep Pasricha, "Run-Time Laser Power Management in Photonic NoCs with On-Chip Semiconductor Optical Amplifiers," IEEE/ACM International Symposium on Networks-on-Chip (NOCS), Nara, Japan, August 2016. **(W--)**

[C7] - Ishan Thakkar, Sai Vineel Reddy Chittamuru, Sudeep Pasricha, "A Comparative Analysis of Front-End and Back-End Compatible Silicon Photonic On-Chip Interconnects," ACM System Level Interconnect Prediction Workshop (SLIP), Austin, TX, USA, June 2016. **(Best Paper Award)** **(W--)**

[C6] - Sai Vineel Reddy Chittamuru, Ishan Thakkar, Sudeep Pasricha, "PICO: Mitigating Heterodyne Crosstalk Due to Process Variations and Intermodulation Effects in Photonic NoCs," IEEE/ACM Design Automation Conference (DAC), Austin, TX, USA, June 2016. (acceptance rate: 152/876=17%) **(W--)**

[C5] - Sai Vineel Reddy Chittamuru, Ishan Thakkar, Sudeep Pasricha, "Process Variation Aware Crosstalk Mitigation for DWDM based Photonic NoC Architectures," IEEE International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, USA, March 2016. (acceptance rate: 36.3%) **(Best Paper Award Finalist)** **(W--)**

[C4] - Ishan Thakkar, Sudeep Pasricha, "Massed Refresh: An Energy-Efficient Technique to Reduce Refresh Overhead in Hybrid Memory Cube Architectures," IEEE International Conference on VLSI Design (VLSID), Kolkata, India, January 2016. (acceptance rate: 86/339 = 25.4%) **(W--)**

[C3] - Ishan Thakkar, Sudeep Pasricha, "A Novel 3D Graphics DRAM Architecture for High-Performance and Low-Energy Memory Accesses," IEEE International Conference on Computer Design (ICCD), New York, NY, USA, Oct 2015. (acceptance rate: 83/269=30.8%) **(W--)**

[C2] - Sudeep Pasricha, Ishan Thakkar, "Re-architecting DRAM memory systems with 3D Integration and Photonic Interfaces," Memory Architecture and Organization Workshop (MeAOW), Oct 2014. **(X)**

[C1] - Ishan Thakkar, Sudeep Pasricha, "3D-Wiz: A Novel High Bandwidth, Optically Interfaced 3D DRAM Architecture with Reduced Random Access Time," IEEE International Conference on Computer Design (ICCD), Seoul, South Korea, Oct 2014. (acceptance rate: 64/207=30.9%) **(W--)**

2.10 Peer-Reviewed PhD Forum

[PF1] - Ishan Thakkar, "Design and Optimization of Emerging Network-Memory Subsystems for Future Manycore Architectures," at the ACM/IEEE Design Automation Conference (DAC) PhD Forum, Austin, TX, USA, June 2017. **(W^{-})**

2.11 Conference Tutorials

[TU1] - A. T-Sanial, Sudeep Pasricha, P. Pande, K. Chakrabarty, "3D Integration: Quo Vadis?" Full-day tutorial at IEEE Design Automation and Test in Europe Conference, (DATE), Mar 2017.
My Contributions: helped with the preparation of the material presented by Sudeep Pasricha.

2.12 Invited Seminar/Conference/Panel Talks

[T10] - Ishan Thakkar, "Towards Petascale In-Package Computing with Unconventional Technologies and Architectures," AI Seminar Series, Oak Ridge National Laboratory, TN, USA, June 2024. **(Z^{+})**

[T9] - Ishan Thakkar, "Evolution of Parallel Architecture Targets: Compilers for Unconventional Computing Architectures," the 36th International Workshop on Languages and Compilers for Parallel Computing (LCPC), Lexington, KY, USA, October 2023. **(Z^{+})**

[T8] - Ishan Thakkar, "Towards Petascale In-Package Computing with Unconventional Technologies and Architectures," Multicore and Multiprocessor SoCs (MPSoCs), Fort Collins, CO, USA, June 2023. **(Z^{+})**

[T7] - Ishan Thakkar, "VBTI Aging: Yet Another Critical Design Challenge for Microring Resonator Based Silicon Photonic Interconnects," Silicon Photonics for High-Performance Computing Workshop (SPHPC), Fort Collins, CO, USA, May 2018. **(Z)**

[T6] - Ishan Thakkar, "Design and Optimization of Interconnection and Memory Subsystems for Future Manycore Computing," Department of Electrical and Computer Engineering, University of Massachusetts Dartmouth, Dartmouth, MA, USA, April 2018. **(Z^{+})**

[T5] - Ishan Thakkar, "Design and Optimization of Interconnection and Memory Subsystems for Future Manycore Computing," Department of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR, USA, March 2018. **(Z^{+})**

[T4] - Ishan Thakkar, "Design and Optimization of Interconnection and Memory Subsystems for Future Manycore Computing," Department of Electrical and Computer Engineering, University of Kentucky, Lexington, KY, USA, February 2018. **(Z^{+})**

[T3] - Ishan Thakkar, "Design and Optimization of Interconnection and Memory Subsystems for Future Manycore Computing," Computer Engineering, Rochester Institute of Technology, Rochester, NY, USA, February 2018. **(Z^{+})**

[T2] – Ishan Thakkar, "Design and Optimization of Interconnection and Memory Subsystems for Future Manycore Computing," Department of Electrical Engineering and Computer Science, University of Kansas, Lawrence, KS, USA, December 2017. **(Z^{+})**

[T1] - Sudeep Pasricha, Ishan Thakkar, “Re-architecting DRAM memory systems with 3D Integration and Photonic Interfaces,” Memory Architecture and Organization Workshop (MeAOW), October, 2014. **(X)***

2.13 Conference Poster Presentations

[CP8] - *Venkata Sai Praneeth Karempudi***, Ishan Thakkar, "Mitigating Inter-Channel Crosstalk Non-Uniformity in Microring Filter Arrays of Wavelength-Multiplexed Photonic NoCs," ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), New York, NY, USA, October 2019. **(W⁻⁻)****

[CP7] - *Supreeth Mysore Shivanandamurthy***, Ishan Thakkar, Sayed Ahmad Salehi, "A Scalable Stochastic Number Generator for Phase Change Memory-Based In-Memory Stochastic Processing," ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), New York, NY, USA, October 2019. **(W⁻⁻)****

[CP6] - *Chao-Hsuan Huang***, Ishan Thakkar, "Mitigating Write Disturbance in Phase Change Memory," ACM/IEEE International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), New York, NY, USA, October 2019. **(W⁻⁻)****

[CP5] - Ishan Thakkar, “Design and Optimization of Emerging Network-Memory Subsystems for Future Manycore Architectures,” in PhD Forum at the ACM/IEEE Design Automation Conference (DAC), Austin, TX, USA, June 2017. **(W⁻⁻)**

[CP4] - Ishan Thakkar, Sai Vineel Reddy Chittamuru, Sudeep Pasricha, "Mitigation of Homodyne Crosstalk Noise in Silicon Photonic NoC Architectures with Tunable Decoupling," ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), Pittsburgh, PA, USA, October 2016. **(W⁻⁻)***

[CP3] - Ishan Thakkar, Sai Vineel Reddy Chittamuru, Sudeep Pasricha, “Run-Time Laser Power Management in Photonic NoCs with On-Chip Semiconductor Optical Amplifiers,” IEEE/ACM International Symposium on Networks-on-Chip (NOCS), Nara, Japan, August 2016. **(W⁻⁻)***

[CP2] - Sai Vineel Reddy Chittamuru, Ishan Thakkar, Sudeep Pasricha, “PICO: Mitigating Heterodyne Crosstalk Due to Process Variations and Intermodulation Effects in Photonic NoCs,” IEEE/ACM Design Automation Conference (DAC), Austin, TX, USA, June 2016. **(W⁻⁻)***

[CP1] - Ishan Thakkar, Sudeep Pasricha, “A Novel 3D Graphics DRAM Architecture for High-Performance and Low-Energy Memory Accesses,” IEEE International Conference on Computer Design (ICCD), New York, NY, USA, October 2015. **(W⁻⁻)***

2.14 Research Posters or Presentations (Non-Conference)

[P13] – *Oluwaseun A. Alo***, Ishan Thakkar, “SPOGA: A Scalable Photonic Accelerator for General Matric Multiplication (GEMM) with Byte-Size Integer Arithmetic,” UKY ECE Research Symposium, April 2024. **(Z+)****

[P12] – *Sairam Sri Vatsavai***, Ishan Thakkar, "SCONNA: A Stochastic Computing Based Optical Accelerator for Ultra-Fast, Energy-Efficient Inference of Mixed Precision Integer-Quantized CNNs," UKY ECE Research Symposium, April 2023. **(Z+)**** **(Best Ph.D. Poster Award)**

[P11] – *David Pippen***, Ishan Thakkar, "Computing with Photonic Phase Change Memory," UKY ECE Research Symposium, April 2023. **(Z+)****

[P10] – *Oluwaseun A. Alo***, Ishan Thakkar, "Silicon Photonics-Based Integer Dot-Product Engine with Configurable Operand Precision," UKY ECE Research Symposium, April 2023. **(Z+)****

[P9] – *Bobby Bose***, Ishan Thakkar, "A Re-configurable Photonic Reduction Network for Deep Neural Network Accelerators," UKY ECE Research Symposium, April 2023. **(Z+)**** **(Best M.S. Poster Award)**

[P8] – *Venkata Sai Praneeth Karempudi***, Ishan Thakkar, "A Hybrid Time-Amplitude Analog Arithmetic Based Optical Accelerator," UKY ECE Research Symposium, April 2023. **(Z+)****

[P7] – *Venkata Sai Praneeth Karempudi***, Ishan Thakkar, "A Polymorphic Electro-Optic Logic Gate for High-Speed Reconfigurable Computing Circuits," UKY ECE Research Symposium, April 2022. **(Z+)****

[P6] – *Sairam Sri Vatsavai***, Ishan Thakkar, "Photonic Reconfigurable Accelerators for Efficient Inference of CNNs With Mixed-Sized Tensors," UKY ECE Research Symposium, April 2022. **(Z+)**** **(Best Ph.D. Poster Award) (Best Signals Poster Award)**

[P5] – *Venkata Sai Praneeth Karempudi***, Ishan Thakkar, "Mitigating Inter-Channel Crosstalk Non-Uniformity in Microring Filter Arrays of Wavelength-Multiplexed Photonic NoCs," ECE Research Symposium, University of Kentucky, Lexington, KY, USA, April 2020. **(Z+)****

[P4] – *Chao-Hsuan Huang***, Ishan Thakkar, "Mitigating the Latency-Area Tradeoffs for DRAM Design with Coarse-Grained Monolithic 3D (M3D) Integration," ECE Research Symposium, University of Kentucky, Lexington, KY, USA, April 2020. **(Z+)****

[P3] – *Chao-Hsuan Huang***, Ishan Thakkar, "Mitigating Write Disturbance in Phase Change Memory Architectures," ECE Research Symposium, University of Kentucky, Lexington, KY, USA, April 2019. **(Z+)****

[P2] - Ishan Thakkar, Sai Vineel Reddy Chittamuru, Sudeep Pasricha, "A Comparative Analysis of Front-End and Back-End Compatible Silicon Photonic On-Chip Interconnects," ACM/IEEE Design Automation Conference Work in Progress (WIP), Austin, TX, USA, June 2016. **(X)***

[P1] - Ishan Thakkar, Sudeep Pasricha, "Improving the Performance and Power Efficiency of Memory with 3D Stacking and High-Bandwidth Optical Interfacing," CSU Ventures Innovation Forum, Fort Collis, CO, USA, April 2016. **(Y)***

2.15 Patents

[PAT4] - U.S. provisional patent application serial no. 63/560,313, titled "Stochastic Computing Enabled Optical Hardware Architectures for Energy-Efficient and Scalable Acceleration of Deep Neural Networks," filed on 03/01/2024.
Inventors: Ishan Thakkar, Sairam Sri Vatsavai, Venkata Sai Praneeth Karempudi

[PAT3] - U.S. provisional patent application serial no. 63/552,415, titled "Charge Domain Computing Inside Dynamic Access Memory," filed on 02/12/2024.
Inventors: Ishan Thakkar

[PAT2] - U.S. Patent, titled "Process-Variability-Based Encryption for Photonic Communication Architectures," US11645382 B2, May 09, 2023.
Inventors: Sai Vineel Reddy Chittamuru, Sudeep Pasricha, Ishan Thakkar

[PAT1] - U.S. provisional patent application serial no. 61/970,155, titled "Low-Cost Chemical and Biochemical Sensor," filed on 3/25/14.
Inventors: Ishan Thakkar, Kevin L Lear, Kenneth F Reardon

3 Educational Activities

3.1 Current Ph.D. Students (Advisor)

[I am looking to hire two graduate students from Fall 2024 / Spring 2025.]

Since August 2022 *Alo Oluwaseun*
Research Topic: Hypergraph Neural Network Acceleration

3.2 Current M.S. Thesis Students (Advisor)

Since July 2022 *David Pippen*
Research Topic: Photonic Integrated Circuits for High-Performance Computing

Since August 2022 *Samrat Patel*
Research Topic: Environmentally Sustainable In-Memory Computing

3.3 Current B.S. Students (Undergraduate Research Advisees)

Since March 2024 *Nathan Turlington*
Research Topic: In-DRAM Computing

Since March 2024 *Christopher Stephens*
Research Topic: In-DRAM Computing

3.4 Past Post-Doc Students (Advisor)

December 2021-May 2022 *Justin Woods* (Co-advised with Dr. Todd Hastings)
Research Topic: Silicon Nitride Optical Modulators

3.5 Ph.D./M.S. Students Graduated (Advisor/Co-Advisor)

May 2024 *Sairam Sri Vatsavai (Ph.D.)*
Dissertation Title: Cross-Layer Design of Highly Scalable and Energy-Efficient AI Accelerator Systems Using Photonic Integrated Circuits

December 2023 *Venkata Sai Praneeth Karempudi (Ph.D.)*
Dissertation Title: Reinventing Integrated Photonic Devices and Circuits for High-Performance Communication and Computing Applications

December 2023 *Bobby Bose (M.S. Thesis)*
Thesis Title: A Flexible Photonic Reduction Network Architecture for Spatial GEMM Accelerators for Deep Learning

May 2023 *Supreeth Mysore Shivanandamurthy (Ph.D.)*

Co-Advisor: Sayed Ahmad Salehi
Dissertation Title: A Phase Change Memory and DRAM-Based Framework for Energy-Efficient and High-Speed In-Memory Stochastic Computing

December 2021 — *Chao-Hsuan Huang (M.S. Thesis)*
Thesis Title: Re-designing Main Memory Subsystems with Emerging Monolithic 3D (M3D) Integration and Phase Change Memory Technologies

3.6 Past B.S. Research Students (Advisor)

April 2020-May 2021 — *Bobby Bose*
Research Topic: DRAM Reliability and In-DRAM Computing
Journal and Conference Publications: C25

3.7 Undergraduate Visiting Scholars

2021-2022 — *Aayushman Ghosh*
Indian Institute of Engineering Science and Technology, Shibpur, India

2020-2021 — *Shreyan Datta*
National Institute of Technology, Durgapur, India
Journal and Conference Publications: C27

3.8 M.S. Project Students Graduated (Supervisor at Colorado State University)

May 2018 — *Varun Kilenje*
Colorado State University
Advisor: Prof. Sudeep Pasricha
Final Project: Exploiting Process Variation to Enhance Hardware Security in Photonic NoC Architectures
Publications: C15, J7

December 2017 — *Rohit Kudre*
Colorado State University
Advisor: Prof. Sudeep Pasricha
Final Project: Reducing Refresh Overhead in Hybrid Memory Cube Architectures with Efficient Power Delivery and Awareness to Inter-Tier Nonuniformity

May 2017 — *Sai Kiran Koppu*
Colorado State University
Advisor: Prof. Sudeep Pasricha
Final Project: Analysis of Front-End and Back-End compatible Silicon Photonic On-Chip Interconnects

3.9 Teaching and Evaluation at the University of Kentucky

(Department teacher/course evaluation average: 4.0 out of 5.0)

Semester	*Course*	*Evaluation*
Spring 2024	EE685-001: Digital Computer Structure	-
Spring 2024	EE/CS/CPE 480: Computer Architecture	-
Fall 2023	EE/CS/CPE 480: Computer Architecture	4.8 out of 5.0
Spring 2023	EE599/699: HW Accelerators for ML	n/a
Spring 2023	EE/CS/CPE 480: Computer Architecture	4.7 out of 5.0
Fall 2022	EE/CS/CPE 480: Computer Architecture	4.7 out of 5.0
Spring 2022	EE576: Cybersecurity	4.6 out of 5.0
Spring 2022	EE/CS/CPE 480: Computer Architecture	3.8 out of 5.0
Fall 2021	EE/CS/CPE 480: Computer Architecture	4.6 out of 5.0
Spring 2021	EE/CS/CPE 480: Computer Architecture	4.1 out of 5.0
Fall 2020	EE685-001: Digital Computer Structure	n/a
Spring 2020	EE599-003: Low Power and Secure Computing	n/a
Spring 2020	EE699-003: Low Power and Secure Computing	n/a
Fall 2019	EE685-001: Digital Computer Structure	4.9 out of 5.0
Spring 2019	EE599-003: HW-SW Design for IoT Systems	4.5 out of 5.0
Spring 2019	EE699-003: HW-SW Design for IoT Systems	4.7 out of 5.0
Fall 2018	EE685-001: Digital Computer Structure	n/a

3.10 Other Teaching Experience

April 2018 — *Guest Lecture*
On the topic of "On-Chip Communication and Interconnection Networks On-Chip (NoCs)" in a graduate level course, Computer Organization and Design, at Colorado State University

October 2017 — *Guest Lecture*
On the topic of "On-Chip Communication: Buses and Networks-on-Chip (NoCs)" in a graduate level course, Hardware-Software Design for Embedded Systems at Colorado State University

September 2016 — *Guest Lecture*
On the topic of "On-Chip Communication: Buses and Networks-on-Chip (NoCs)" in a graduate level course, Hardware-Software Design for Embedded Systems, at Colorado State University

August 2016 — *Guest Lecture*
On the topic of "System C Tutorial" in a graduate level course, Hardware-Software Design for Embedded Systems, at Colorado State University

October 2015	*Guest Lecture* On the topic of "On-Chip Communication: Buses and Networks-on-Chip (NoCs)" in a graduate level course, Hardware-Software Design for Embedded Systems, at Colorado State University
Fall 2015	*Teaching Assistant* For a graduate-level course, Computer Organization and Design
Fall 2011	*Teaching Assistant* Taught assembly-level programming to junior students in an undergraduate course, Introduction to Microprocessors
Spring 2011	*Teaching Assistant* For a graduate-level course, Engineering Risk Analysis
Summer 2010	*Expert Lectures* On "Preparing for Quantitative Aptitude Tests" to senior-level undergraduate students at Genesis Consultants, Institute for Management and Foreign Studies (IMFS), India
Fall 2009 Spring 2010	*Ad-hoc Lecturer* Taught "Basics of Programming using C and C++" and "Elements of Electrical Engineering" to sophomore undergraduate students at the Venus International College of Technology (VICT), Gandhinagar, Gujarat, India
September 2010	*Expert Lecture* On the topic of "Robust Hardware Design for Remotely Controlled Robocars" to undergraduate students at the Venus International College of Technology (VICT), Gandhinagar, Gujarat, India

3.11 Student Awards

2023	*Travel Award*, IEEE Technical Community on Parallel Processing (TCPP) award to travel to the IEEE IPDPS 2023 conference (*Sairam Sri Vatsavai*)
2023	*Best M.S. Poster Award*, UKY ECE Research Symposium (*Bobby Bose*)
2023	*Best Ph.D. Poster Award*, UKY ECE Research Symposium (*Sairam Sri Vatsavai*)
2022	*Best Signals Poster Award*, UKY ECE Research Symposium (*Sairam Sri Vatsavai*)
2022	*Best Ph.D. Poster Award*, UKY ECE Research Symposium (*Sairam Sri Vatsavai*)
2020	*Student Participation Support*, IEEE IGSCC 2020 (*Supreeth Shivanandamurthy*)
2020	*Student Participation Support*, IEEE IGSCC 2020 (*Venkata Sai Praneeth Karempudi*)
2020	*Student Participation Support*, IEEE IGSCC 2020 (*Sairam Sri Vatsavai*)
2020	*Student Participation Support*, IEEE IGSCC 2020 (*Chao-Hsuan Huang*)

2019	*Travel Award*, ACM/IEEE ESWEEK 2019 (*Chao-Hsuan Huang*
2019	*Travel Award*, ACM/IEEE ESWEEK 2019 (*Supreeth Mysore Shivanandamurthy*
2019	*Travel Award*, ACM/IEEE ESWEEK 2019 (*Venkata Sai Praneeth Karempudi*)

3.12 Professional Development (Participation)

April 2023	*NSF CISE CAREER Workshop* Zoom Webinar, National Science Foundation
March 2019	*NSF CAREER Workshop* Proposal Development Office, University of Kentucky Research Foundation, Lexington, KY, USA
June 2017	*DAC Early Career Workshop* IEEE/ACM Design Automation Conference (DAC), Austin, TX, USA
June 2017	*Entering Mentoring* Certificate course at Colorado State University, Fort Collins, CO, USA
May 2017	*NSF Day Workshop* University of Wyoming, Laramie, WY, USA
April 2015	*Interacting with Federal Funding Agencies* Seminar at the Information Science and Technology Center (ISTeC), Colorado State University, Fort Collins, CO, USA

4 Professional and University Service

4.1 ACM/IEEE Executive Committees

Since 2021 *Social Media Co-Chair*
ACM Special Interest Group on Design Automation (SIGDA)

4.2 Editorial Activities

Since 2024 *Guest Editor*
Special Issue "Memory Technologies for HPC/AI Workloads: Device-Level Innovations to System-Level Optimizations (VSI: HPC/AI)" in the Elsevier Memories - Materials, Devices, Circuits and Systems Journal

Since 2021 *Associate Editor*
IEEE Technical Committee on Very Large-Scale Integration (TCVLSI) Newsletter

2021-2022 *Review Editor*
Frontiers in Neuroscience Journal, Editorial Board of Neuromorphic Engineering

4.3 Proposal Review Panels

2024 National Science Foundation (Two Panels – One SaTC and One CISE Special Program)

2022 National Science Foundation (One CISE Core Panel)

2020 National Science Foundation (One CISE Core Panel)

4.4 Conference/Workshop Organizing Committee (General/Program Chair)

2024 *Program Chair*
10th IEEE International Symposium on Smart Electronic Systems (IEEE-iSES)

2020 *General Chair*
Workshop on Computing with Unconventional Technologies (CUT),
Co-located with International Green and Sustainable Computing (IGSC) Conference

2019 *General Chair*
Workshop on Computing with Unconventional Technologies (CUT),
Co-located with International Green and Sustainable Computing (IGSC) Conference

4.5 Conference/Workshop Organizing Committee (Other Chaired Positions)

2023 *Lead Scribe*
NSF Workshop Series on Sustainable Computing (SUSCOMP)

2023 *Workshop Co-Chair*
IEEE International Green and Sustainable Computing (IGSC) Conference

2022 *Workshop Co-Chair*
IEEE International Green and Sustainable Computing (IGSC) Conference

2021 *Workshop Co-Chair*
IEEE International Green and Sustainable Computing (IGSC) Conference

2020 *Virtual Conference Management Chair*
IEEE International Green and Sustainable Computing (IGSC) Conference

2020 *Panel Chair, Moderator*
IEEE/ACM International Workshop on Network on Chip Architectures (NoCArc)

2020 *Web Chair*
IEEE/ACM International Symposium on Networks-on-Chip (NOCS)

2019 *Web Chair*
IEEE/ACM International Symposium on Networks-on-Chip (NOCS)

2017 *Publicity Chair*
IEEE International Green and Sustainable Computing (IGSC) Conference

4.6 Conference Technical Program Committee (TPC) Member

[150+ papers reviewed]

2024 IEEE/ACM International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES) [Reviewed 7 Papers]

2024 IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) [Reviewed 5 Papers]

2024 ACM Great Lakes Symposium on VLSI (GLSVLSI)

2024 IEEE International Symposium on Quality Electronic Design (ISQED)

2023 IEEE International System-On-Chip Conference (SOCC)

2023 IEEE/ACM International Symposium on Networks-on-Chip (NOCS)

2023 ACM Great Lakes Symposium on VLSI (GLSVLSI)

2023 IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)

2023 IEEE International Symposium on Quality Electronic Design (ISQED)

2022 IEEE/ACM International Workshop on Network on Chip Architectures (NoCArc)

2022 ACM Great Lakes Symposium on VLSI (GLSVLSI)

2022 IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)

2022 IEEE International Symposium on Quality Electronic Design (ISQED)

2022	IEEE/ACM Design Automation Conference (DAC)
2021	IEEE/ACM International Workshop on Network on Chip Architectures (NoCArc)
2021	ACM/IEEE Design Automation Conference (DAC) Late Breaking Results (LBR)
2021	IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)
2021	IEEE/ACM International Symposium on Networks-on-Chip (NOCS)
2021	IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)
2021	IEEE International Symposium on Quality Electronic Design (ISQED)
2021	ACM/IEEE Design Automation Conference (DAC)
2020	IEEE International Green and Sustainable Computing (IGSC) Conference
2020	IEEE/ACM International Symposium on Networks-on-Chip (NOCS)
2020	ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)
2020	ACM Great Lakes Symposium on VLSI (GLSVLSI)
2020	ACM/IEEE Design Automation Conference (DAC)
2019	IEEE International Green and Sustainable Computing (IGSC) Conference
2019	IEEE International Symposium on Embedded Many-core Systems-on-Chip (MCSoC)
2019	IEEE/ACM International Symposium on Networks-on-Chip (NOCS)
2019	ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)
2019	IEEE International Conference on VLSI Design
2018	IEEE International Green and Sustainable Computing (IGSC) Conference
2018	IEEE International Conference on VLSI Design
2017	IEEE International Green and Sustainable Computing (IGSC) Conference

4.7 Activities as a Journal Reviewer/Conference External Reviewer

[50+ manuscripts reviewed through multiple review stages]

2024-Present	Nature Communications (Early Career Co-Reviewer)
2023-Present	IEEE Letters of Photonics Technology
2023-Present	Elsevier Journal of Optics and Laser Technology
2021-Present	IEEE Embedded Systems Letters
2020	IEEE Computer Society Annual Symposium on VLSI (ISVLSI)
2020-Present	IEEE Computer Architecture Letters
2020-Present	IEEE Transactions on Computers (TC)
2020-Present	Elsevier Journal of Sustainable Computing: Informatics and Systems

2019-Present	ACM Transactions on Architecture and Code Optimization (TACO)
2019	IEEE/ACM Design and Automation Conference (DAC)
2018-Present	Elsevier Journal of Parallel and Distributed Computing
2018-Present	Springer Design Automation for Embedded Systems
2018	IEEE/ACM Design and Automation Conference (DAC)
2017	IEEE/ACM Design Automation Conference (DAC)
2016-Present	IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
2016	IEEE/ACM International Symposium on Networks-on-Chip (NOCS)
2016-Present	ACM Transactions on Embedded Computing Systems
2015-Present	IEEE Transactions on Multi-Scale Computing Systems
2015-Present	IEEE Transactions on Very Large-Scale Integration Systems
2015-Present	ACM Transactions on Design Automation of Electronic Systems (TODAES)
2014-Present	ACM Journal on Emerging Technologies in Computing Systems

4.8 Activities as a Referee of Research Forums

2020 *Referee of Student Research Forum*
IEEE International Green and Sustainable Computing (IGSC) Conference

2020 *Referee of ACM SIGDA / IEEE CEDA Ph.D. Forum*
ACM/IEEE Design Automation Conference (DAC)

2018 *Referee of Student Research Forum*
IEEE International Green and Sustainable Computing (IGSC) Conference

4.9 Conference Technical Session Chair

2023 ACM Great Lakes Symposium on VLSI (GLSVLSI)

2022 ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)

2021 ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)

2021 IEEE/ACM International Symposium on Networks-On-Chip (NOCS)

2020 IEEE/ACM Design Automation Conference (DAC)

2019 ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)

2019	IEEE/ACM International Symposium on Networks-on-Chip (NOCS)

4.10 University, College, and Department Service

2024	Judge at the ECE Research Symposium, Electrical and Computer Engineering Department, University of Kentucky, Spring 2024
2023-2024	Member of Computer Engineering Faculty Search Committee, Electrical and Computer Engineering Department, University of Kentucky
2023	Judge at the ECE Research Symposium, Electrical and Computer Engineering Department, University of Kentucky, Spring 2023
2022	Judge at the ECE Research Symposium, Electrical and Computer Engineering Department, University of Kentucky, Spring 2022
2022-Present	Member of ECE Undergraduate Committee, Electrical and Computer Engineering Department, University of Kentucky
2021	Judge at the ECE Research Symposium, Electrical and Computer Engineering Department, University of Kentucky, Spring 2021
2021	Nominated Member of Computer Engineering Graduate Committee, College of Engineering, University of Kentucky
2021-Present	Faculty of Cybersecurity Certificate Program, College of Engineering, University of Kentucky
2019-2020	Member of Strategic Planning Committee, Electrical and Computer Engineering Department, University of Kentucky